PennState

MURI Device Design and Testing for Collaborative Research on Radiation effects

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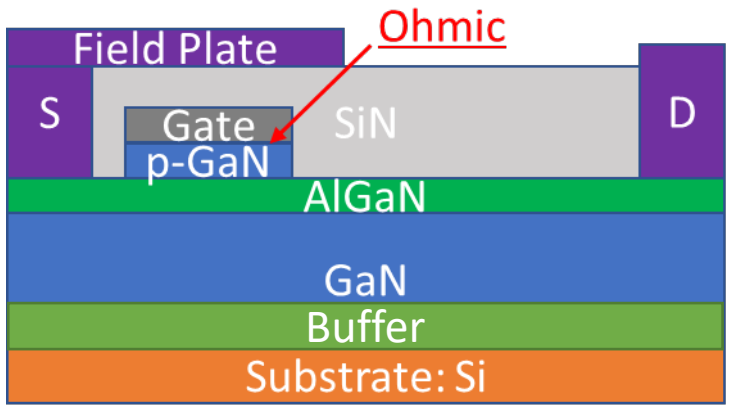
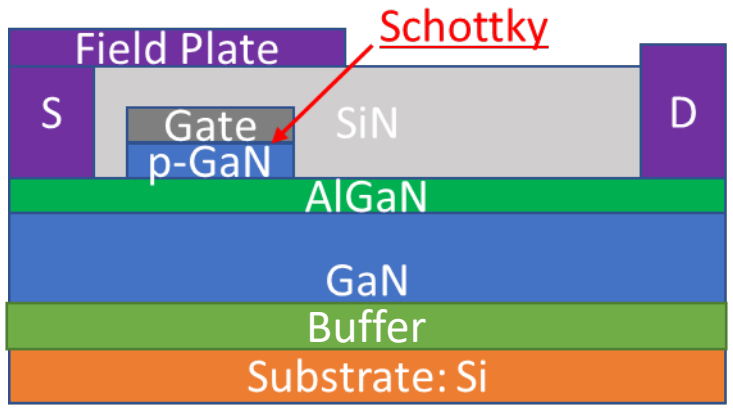
Background

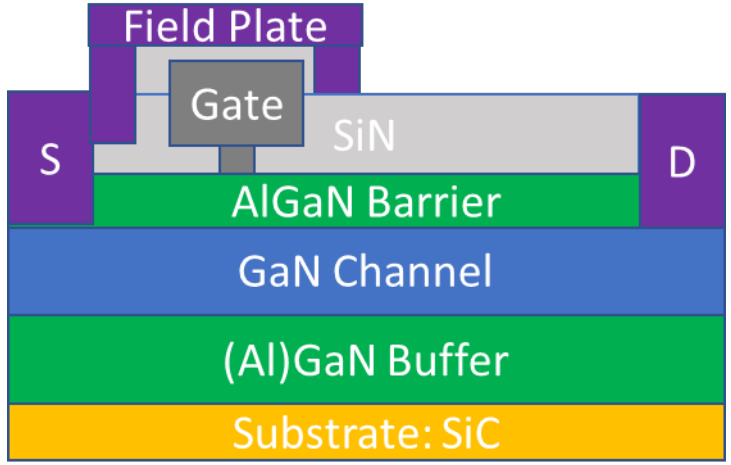
❑ **Objective: baseline device test structures to reveal radiation physics and drive collaboration**



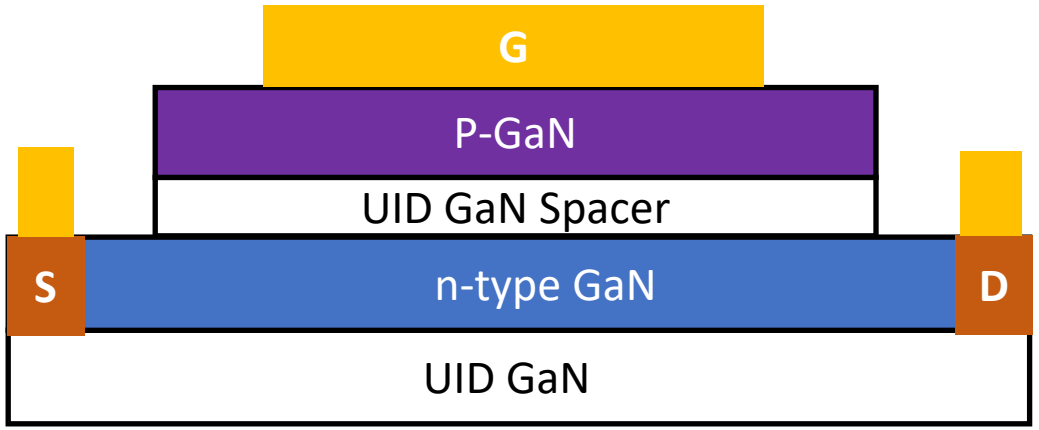
Power HEMTs: Panasonic, Infineon, …



Power HEMTs: EPC, TSMC, …



RF HEMTs: Wolfspeed, Qorvo, …

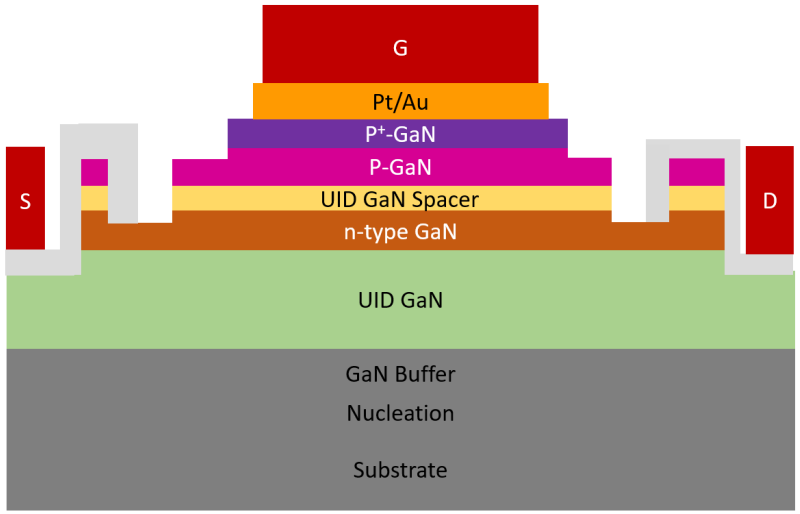


❑ **JFET as basic test structure:**

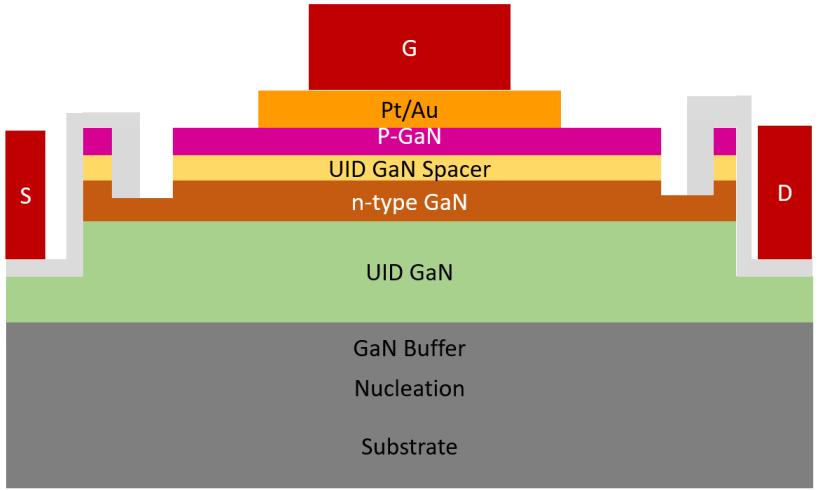
- ❑ **Start with no-AlGaN structure for simplicity.**
- ❑ **Can also be tested as a PN diode.**

Batch 1 Device structure splits

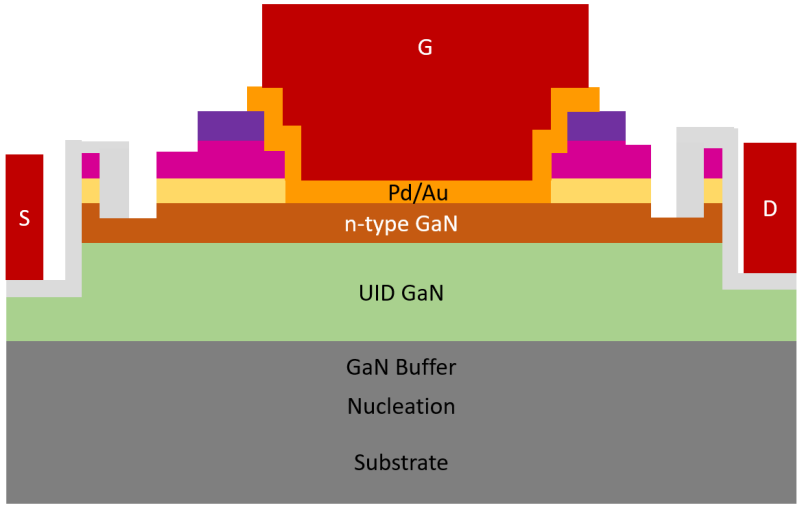
- Three gate variations based on baseline and commercial gate structures.



P-GaN Gate JFET



P-GaN Gate JFET, Schottky to P-GaN

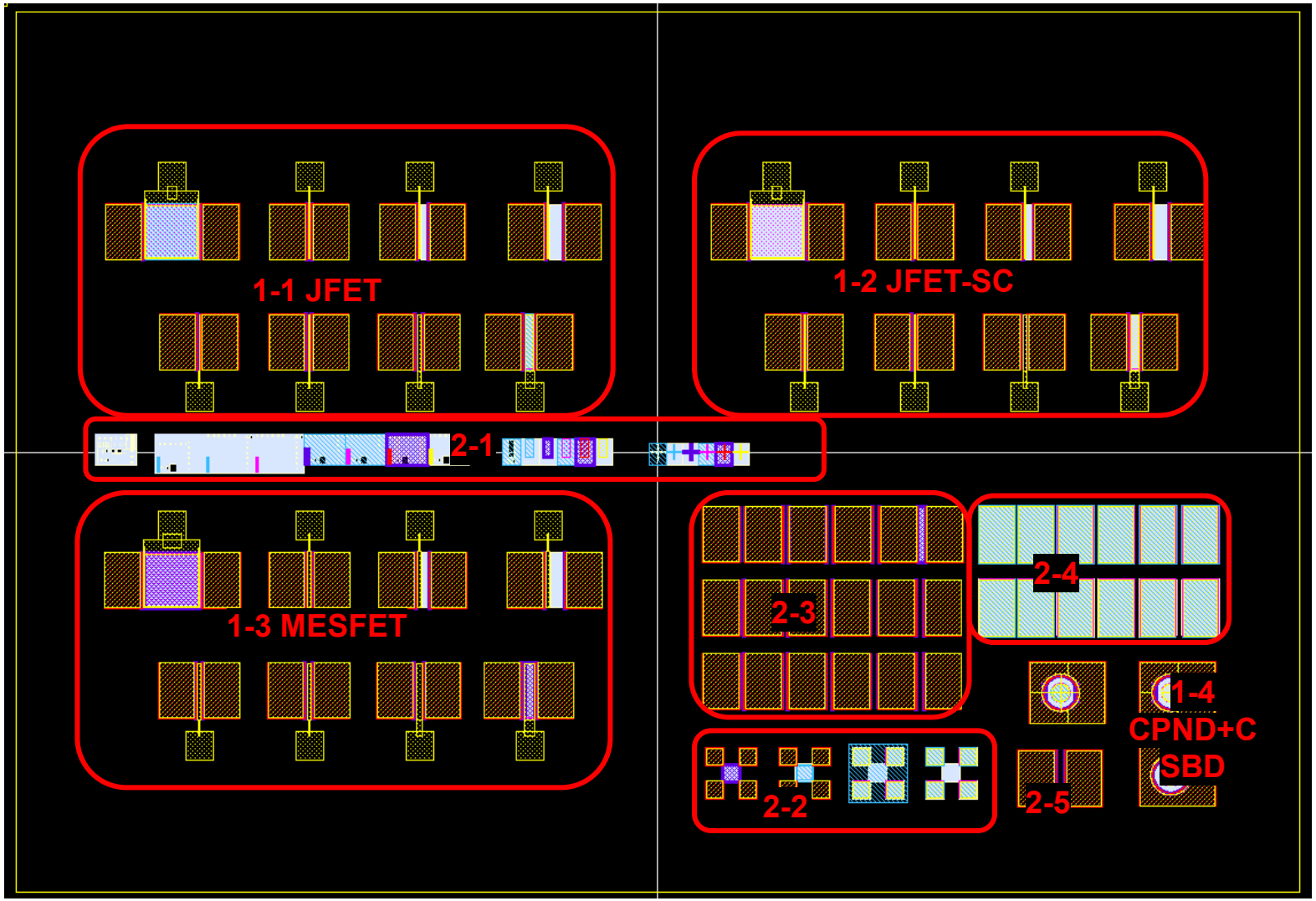


MESFET

- Considerations for spectroscopy:
  - Magnetic resonance: Avoid magnetic materials, e.g., Ni.
  - DLOS: “Semi-transparent” metallization

Batch 1 Layout

❑ Die Size = 7mm x 4.8mm



❑ Device arrangement

Transistors:

1-1: JFET: L_{JTE}=4, 10, 40, 80um:

L_{Gate}=2, 10, 20, 50, 300um

1-2: JFET-SC: L_{JTE}=4, 10, 40, 80um: L_{Gate}=2, 10, 20, 50, 300um

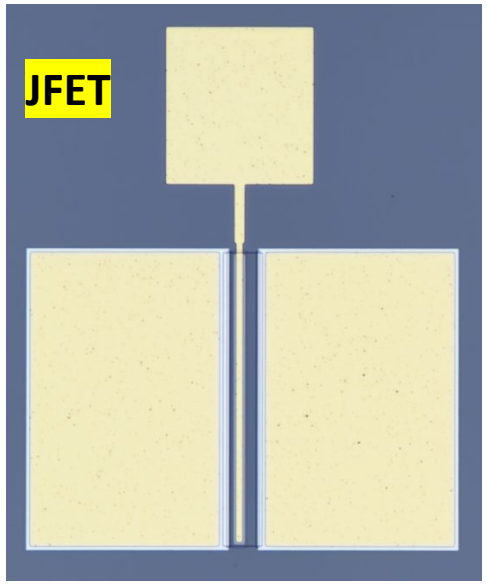
1-3: MESFET: L_{JTE}=4, 10, 40, 80um: L_{Gate}=2, 10, 20, 50, 300um

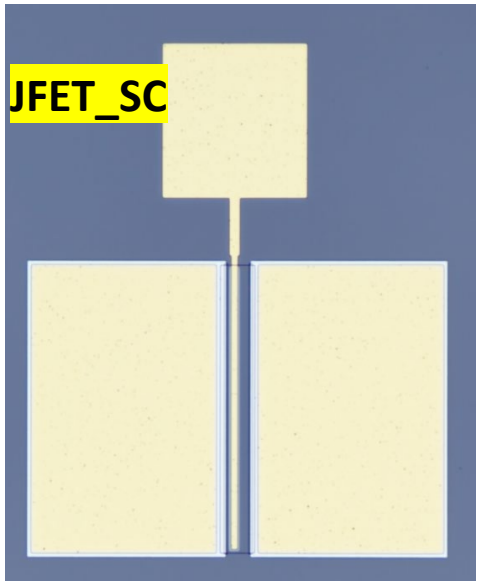
Test structures:

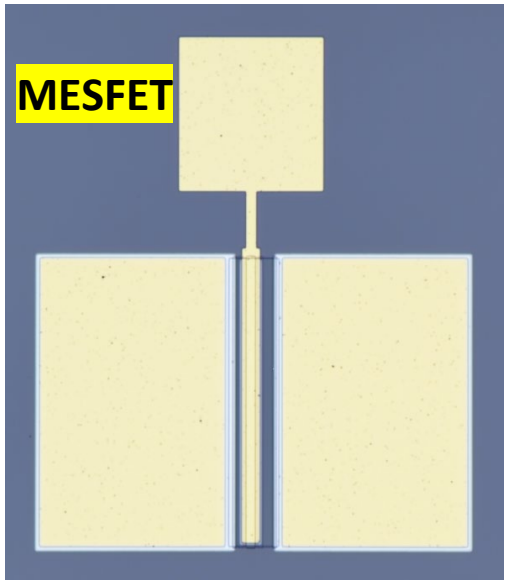
1-4: CPND: Ohmic and Schottky PGaN, CSBD. L_{JTE}=40um

2-1: Inspection Patterns
2-2: Hall Effect
2-3: N -LTLM
2-4: P -LTLM
2-5: Isolation: L_{gap} = 40 um

Batch 1 Representative Devices



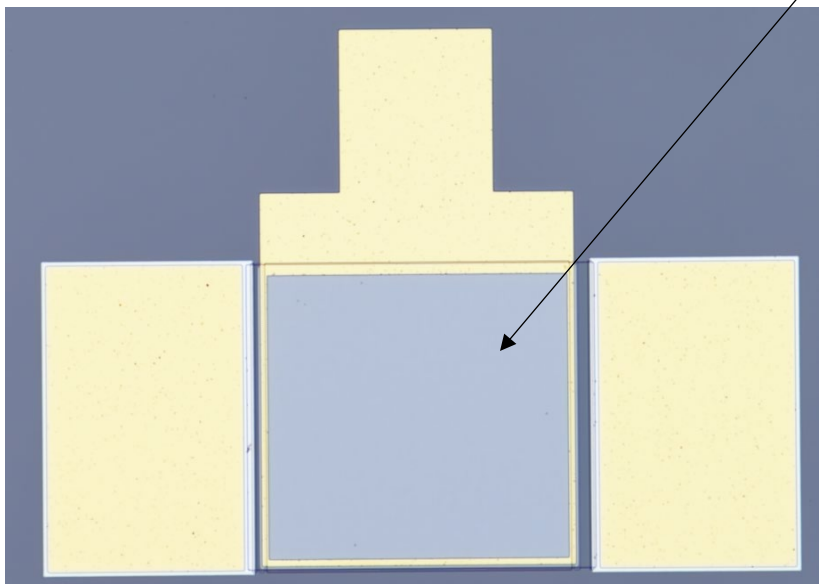




L_g=10 um

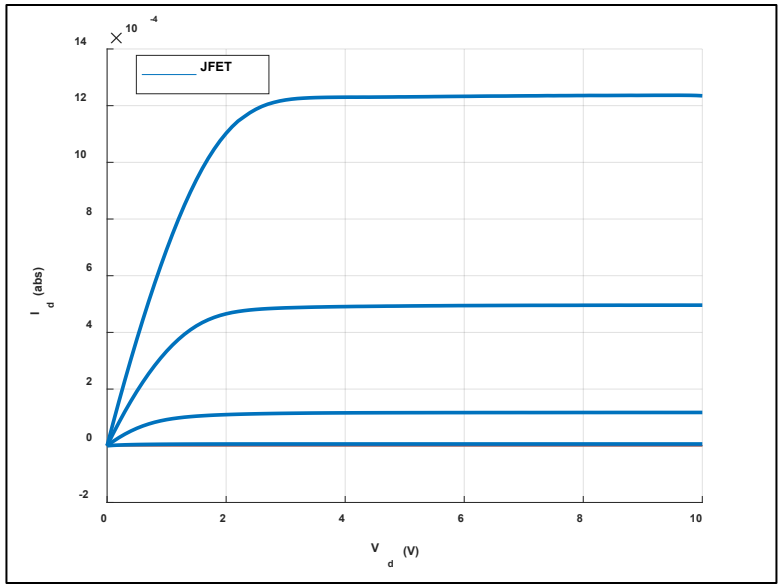
L_{JTE}=10 um

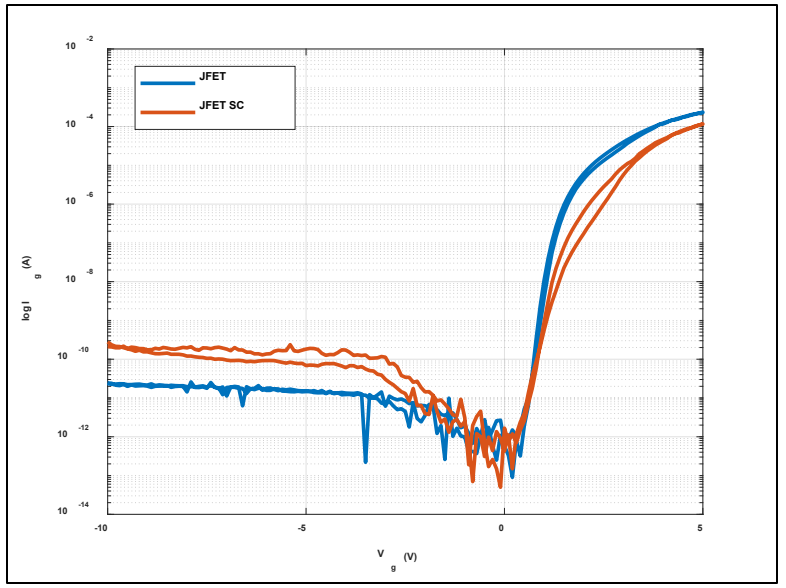
- Sample size:
  - ¼ of a 4 inches wafer
  - ~40 dies in 1 sample

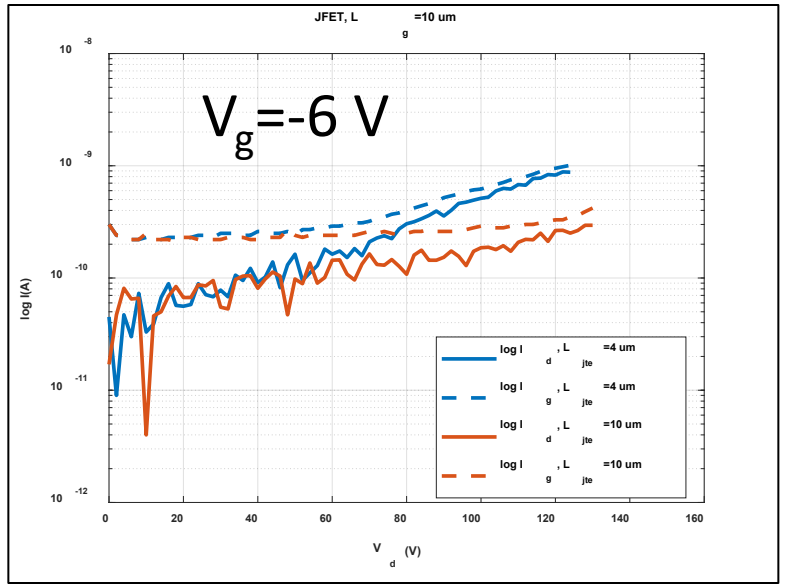


MESFET with 300 um gate

Batch 1 Electrical Results







Magnetic Resonance on Batch 1

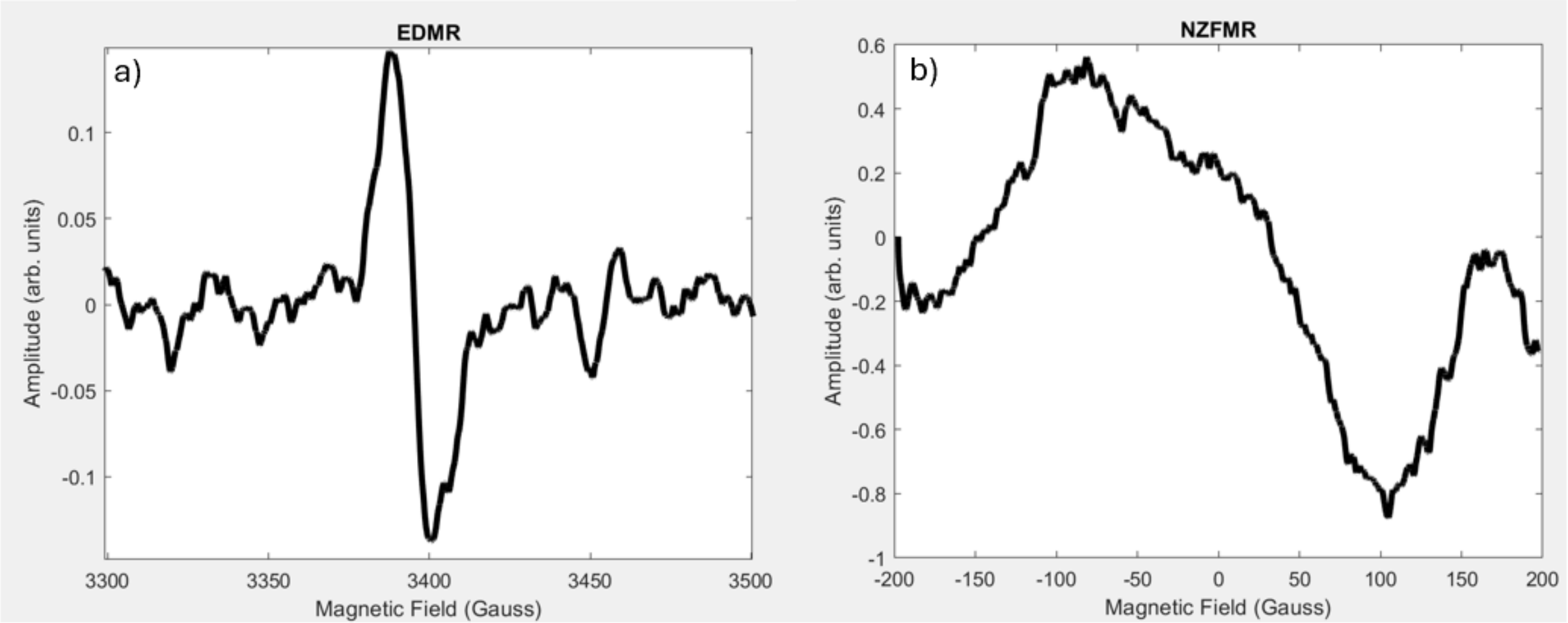


Figure 2. We show a) an EDMR response and b) an NZFMR response on a GaN pn junction diode fabricated by Dr. Chu's group.

Batch 1 Irradiation

Many thanks to Prof. Maik Lang, Dr. Eric Quinn & Dr. Voss, Kay-Obbe & GSI members

GSI – Ar ion on-site

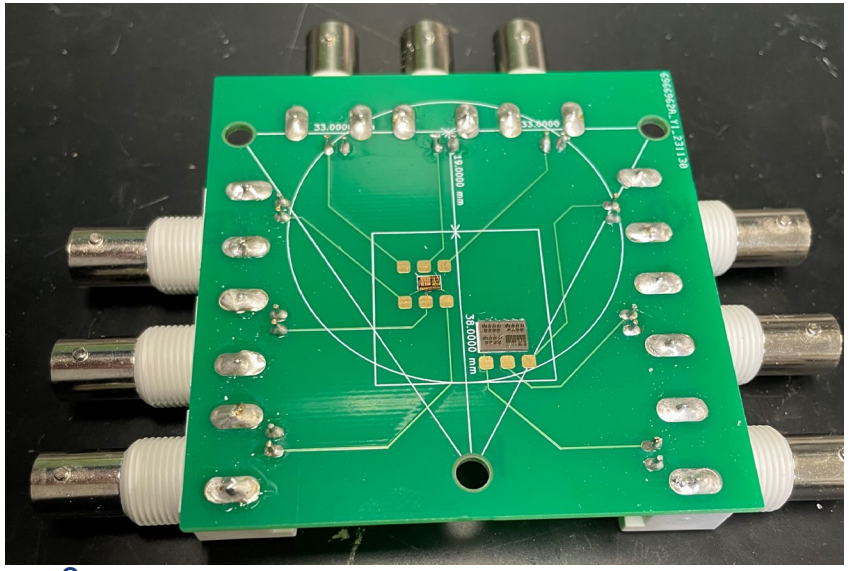
Ion	Energy	Range	LET (MeV/(mg/cm^2))
^{40}Ar	192 MeV (4.8 MeV/u)	26 µm	10.8

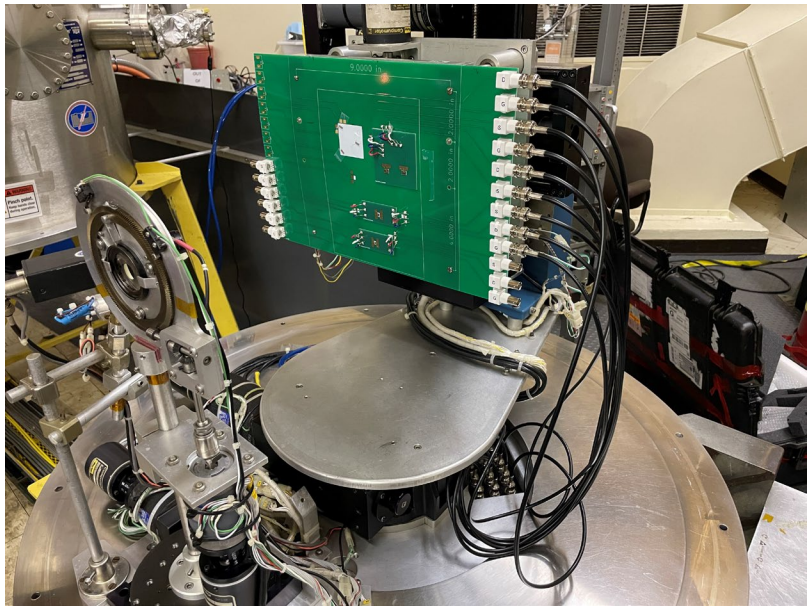
BNL – Au ion on-site

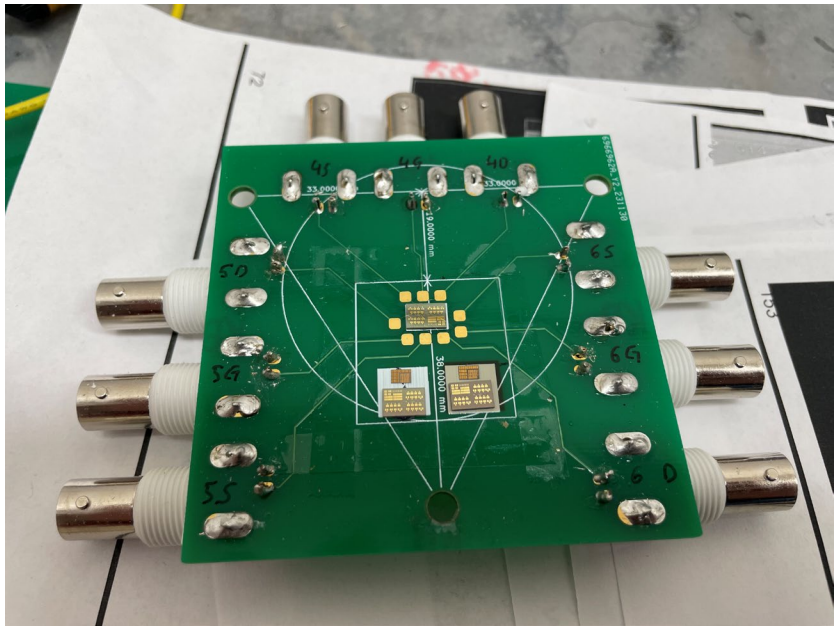
Ion	Energy	Range	LET (MeV/(mg/cm^2))
^{197}Au	333.7 MeV (1.71 MeV/u)	27.6 µm	81.47

GSI – Au ion

Ion	Energy	Range	LET (MeV/(mg/cm^2))
^{197}Au	950 MeV (4.8 MeV/u)	30 µm	72.4



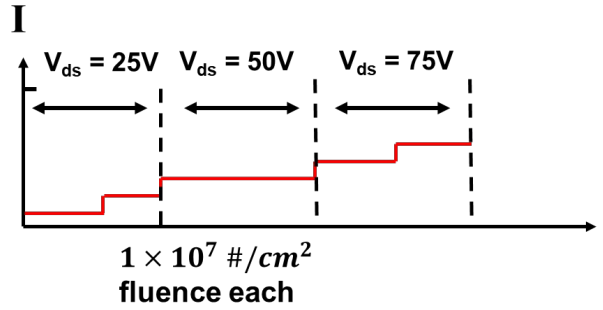


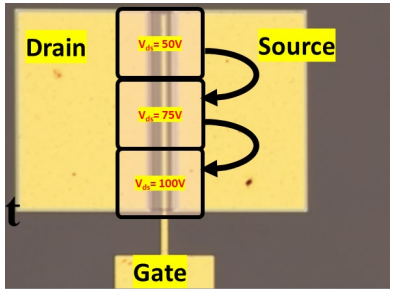


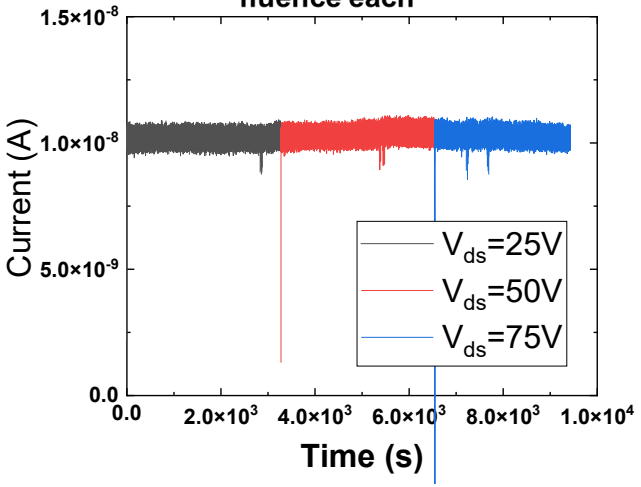
Batch 1 Testing Under Irradiation

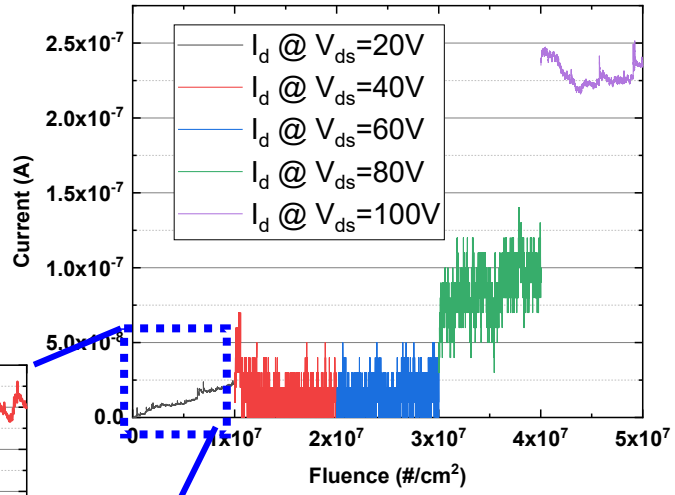
Ion	Energy	Range	LET
^{40}Ar	192 MeV	26 μm	10.8 MeV/(mg/cm^2)

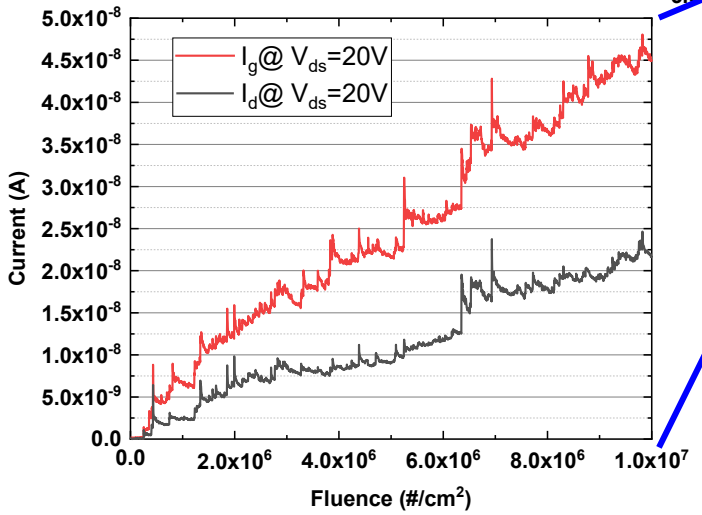
Ion	Energy	Range	LET
^{137}Au	333.7 MeV	27.6 μm	81.47 MeV/(mg/cm^2)

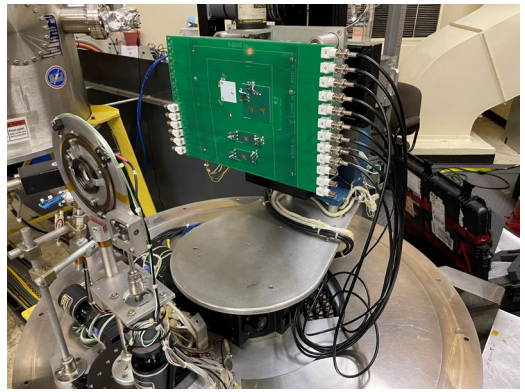








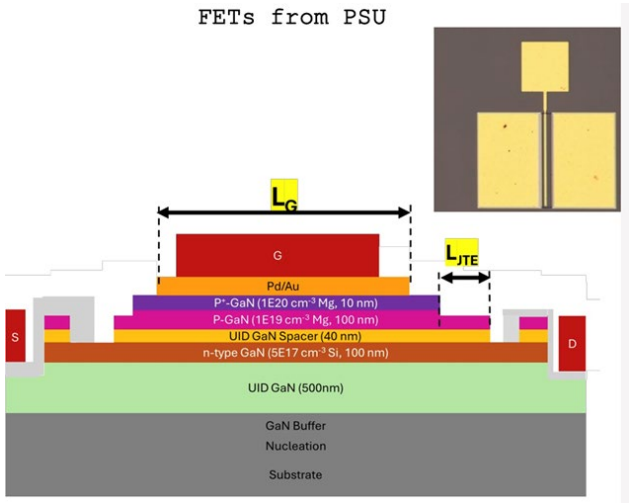


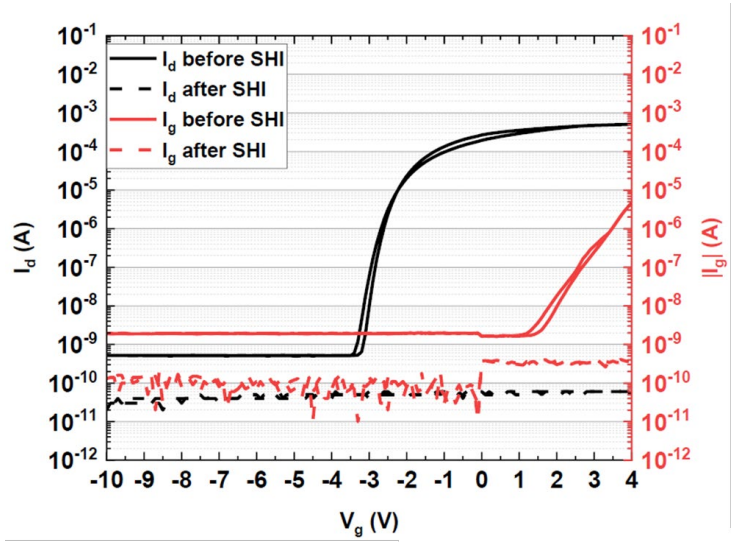


Rongming Chu Group

In Collaboration with Maik Lang Group

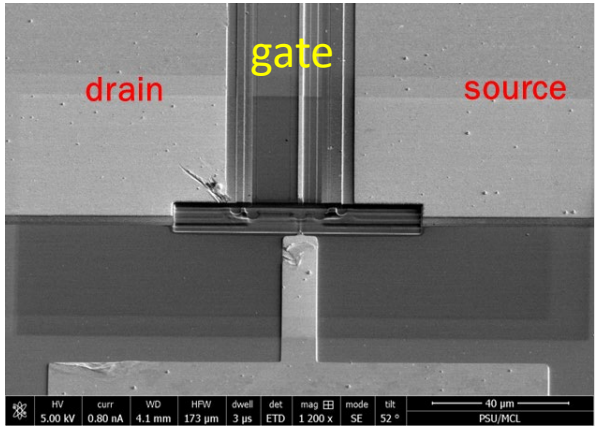
Batch 1 Testing Before & After Irradiation

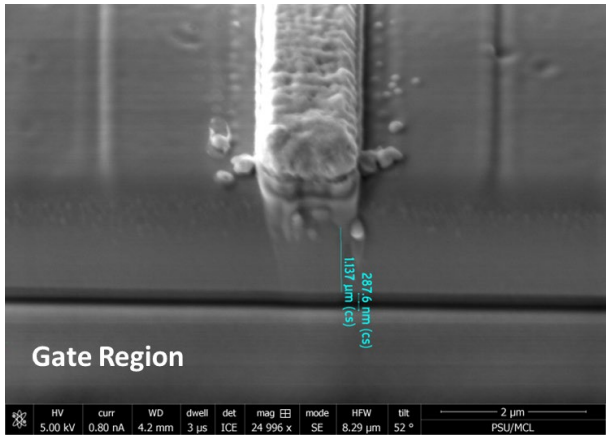


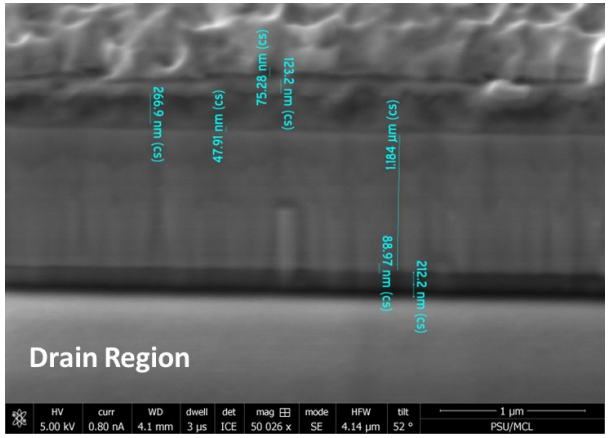


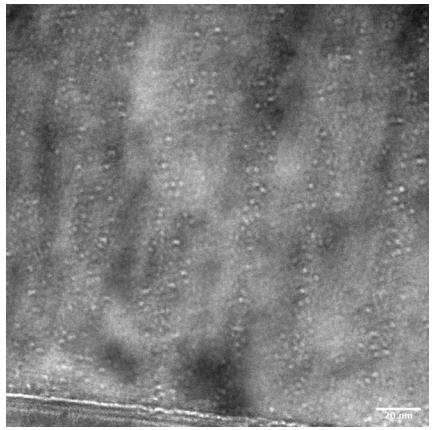
Ion	Energy	Range	LET
^{137}Au	950 MeV	30 µm	72.4 MeV/(mg/cm^2)

5×10^{11} ions/cm^2

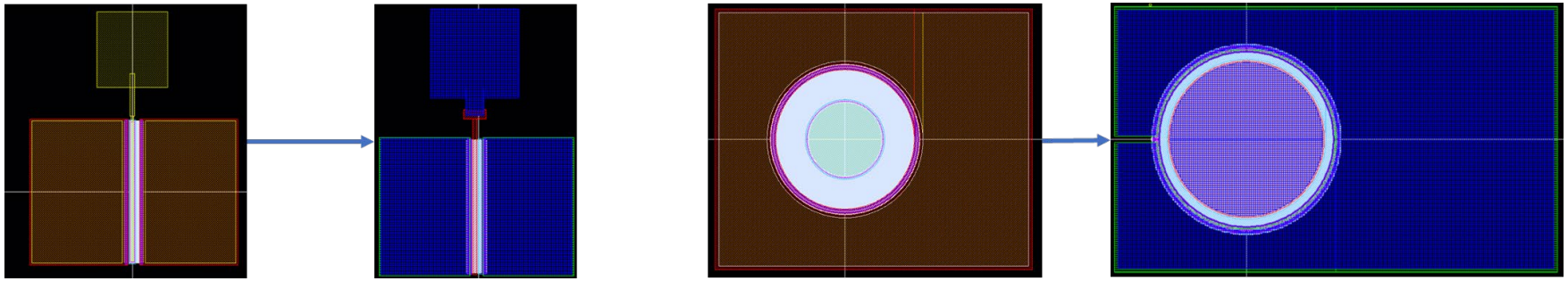


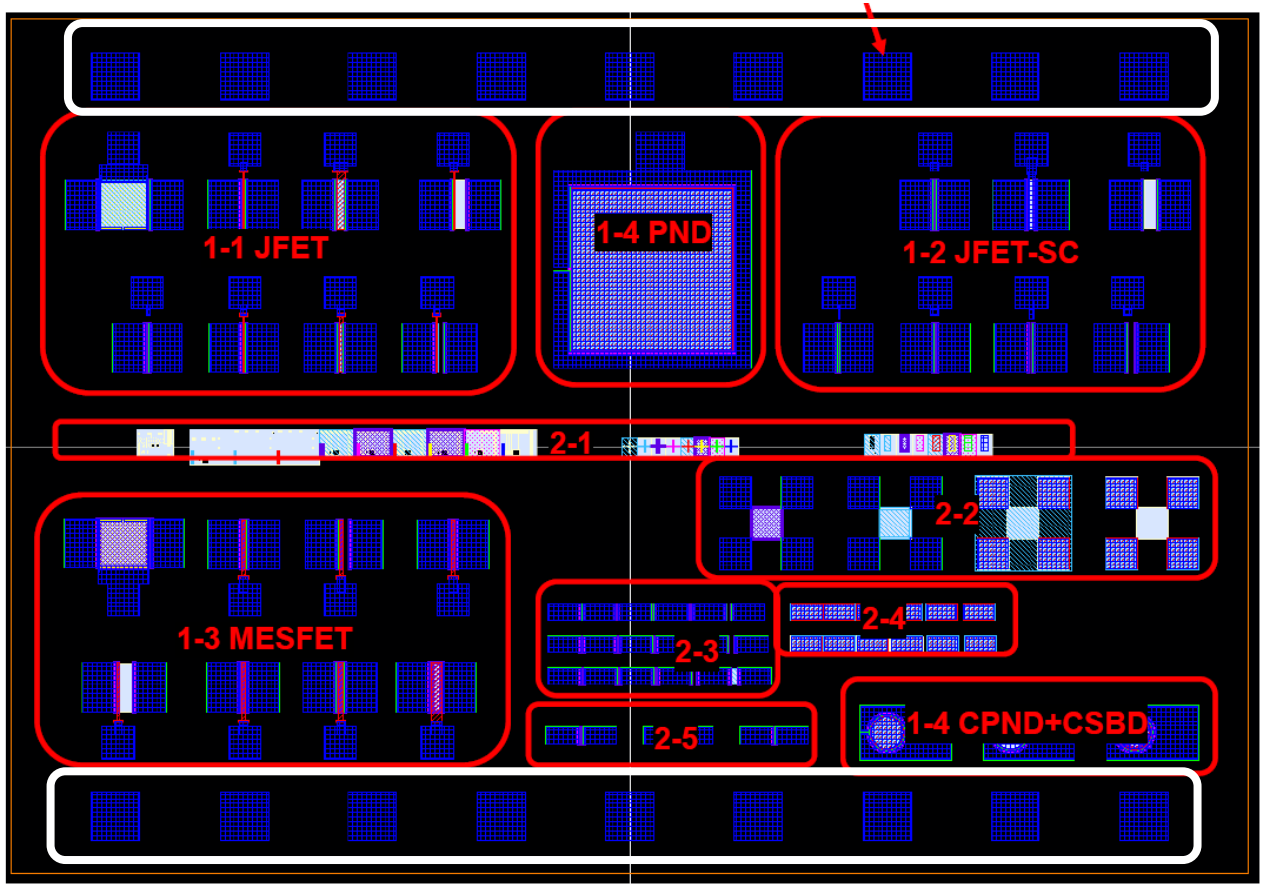






Batch 1 -> Batch 2: Design Improvements



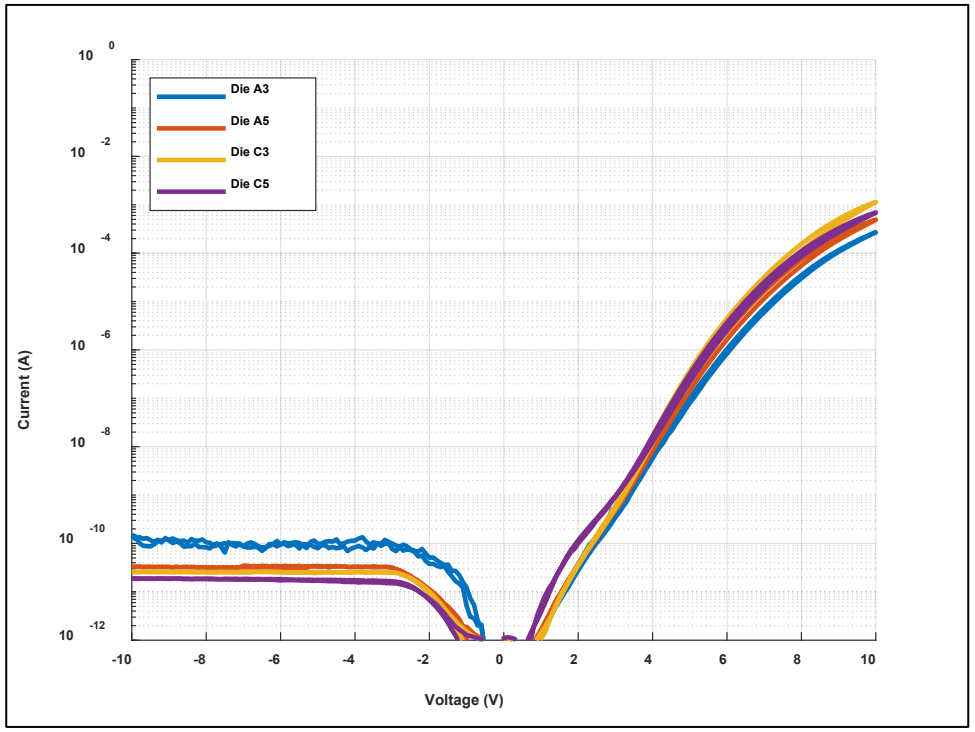


Split P-ohmic into 2 layers

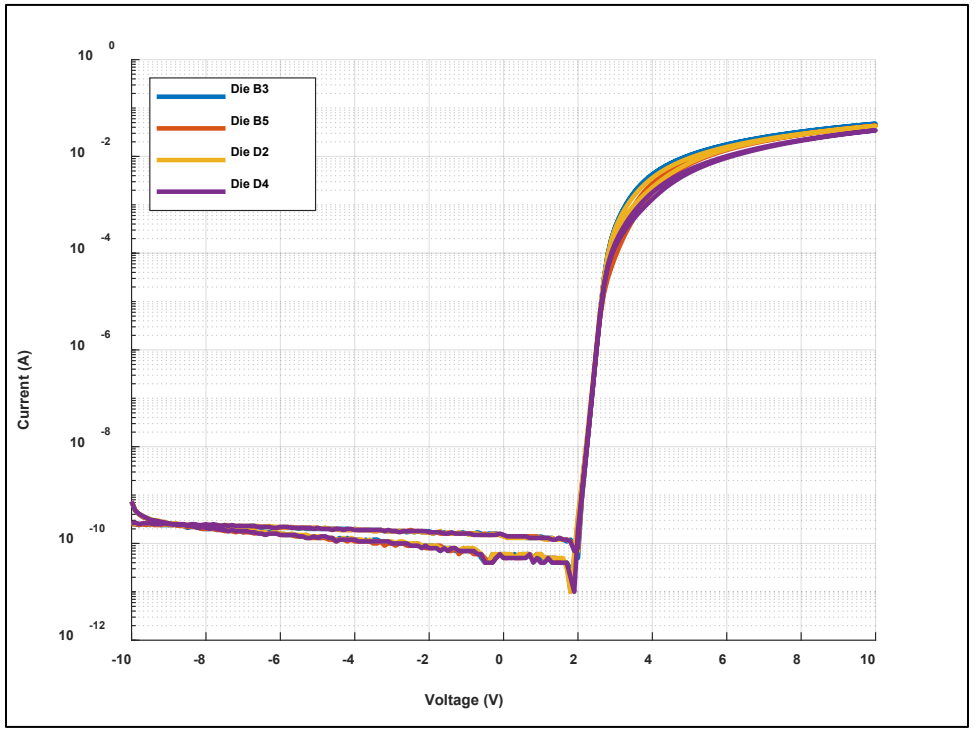
P-Ohmic for 300 um gate JFET/MESFET	Pd/Au (50/50 Å)
P-Ohmic for all other devices	Pd/Au (400/1000 Å)

Batch 2: Design Improvements

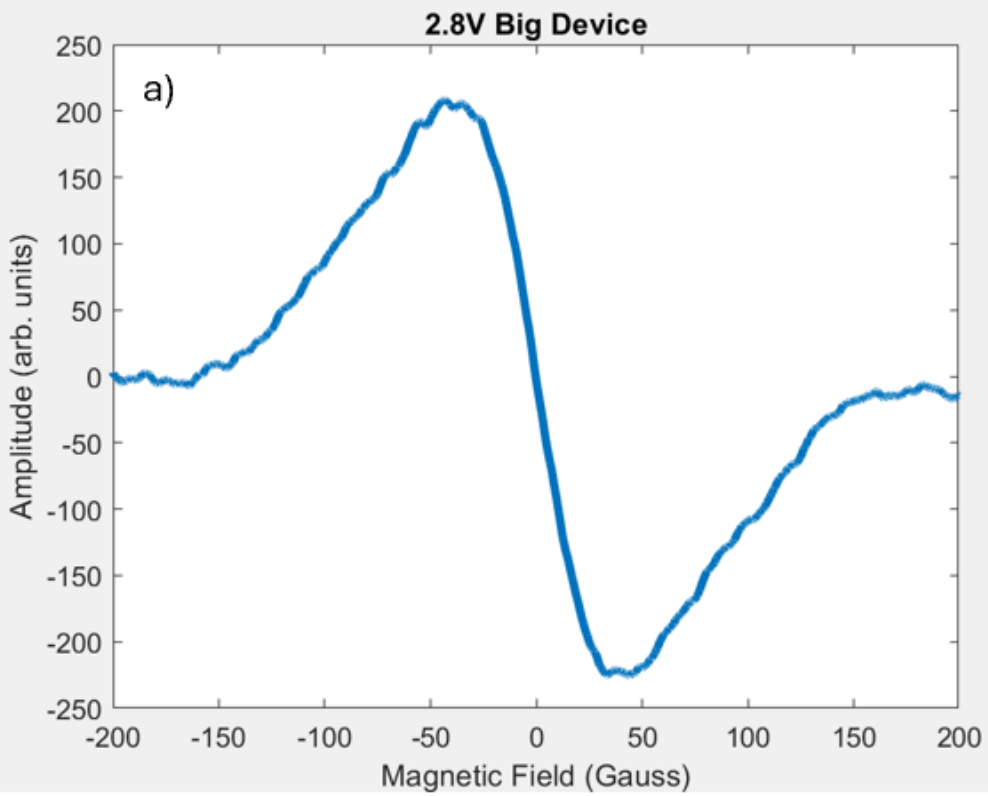
1st Batch



2nd Batch



Magnetic Resonance on Batch 2



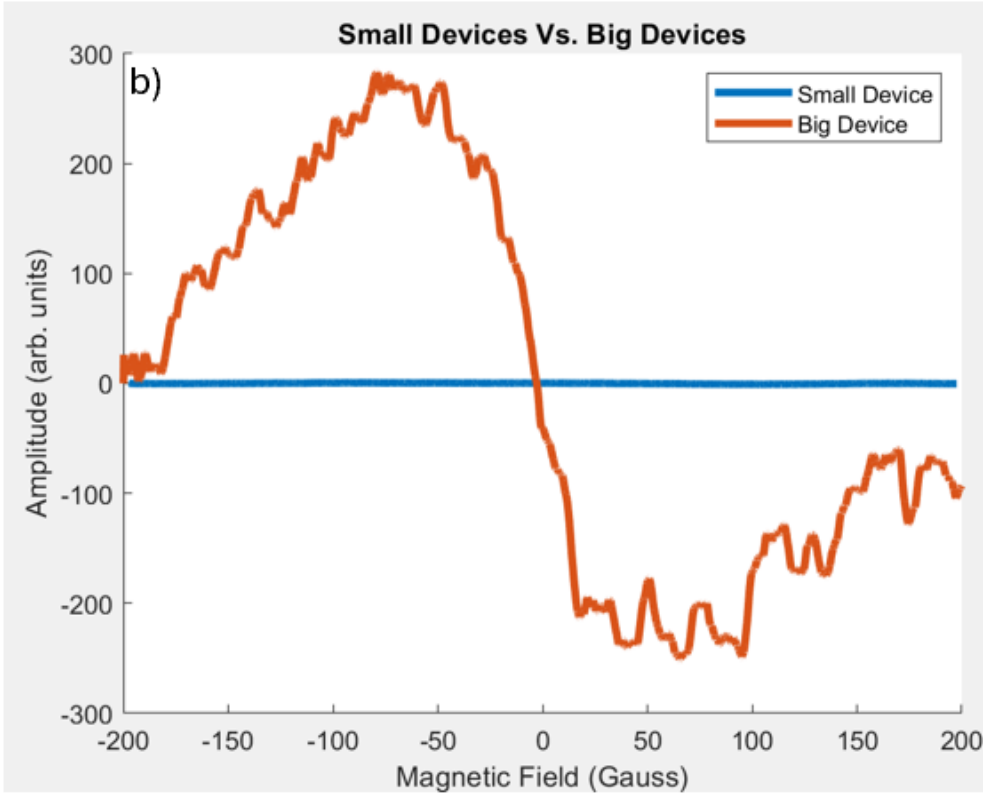


Figure 3. In a), we show an NZFMR response on a much larger device recently provided by Dr. Chu's group. The cross-sectional area of this device is about 1mm^2. In b), we illustrate a comparison between the measurements in the new larger devices and the earlier smaller device provided by Dr. Chu's group (as illustrated in Figure 2). The two traces were chosen to match as closely as possible spectrometer settings and device biasing conditions.

Summary

Year 2

- ✓ **Simulated and characterized cavities caused by heavy ions.**
- ✓ **Magnetic resonance signals and interpretations.**
- ✓ **Heavy ion causes junction leakage, no device failure yet**

Questions

- ❑ **What is the correlation between structural defects and leakage?**
- ❑ **What is the impact of additional leakage on long-term reliability?**
- ❑ **What if we insert an AlGaN layer into the device structure?**
- ❑ **What will cause single-event device failure: dielectrics? Si substrate?**