Novel III-V Growth Technologies - Alternative Growth Technologies, Templates and/or Epitaxial Removal Technologies

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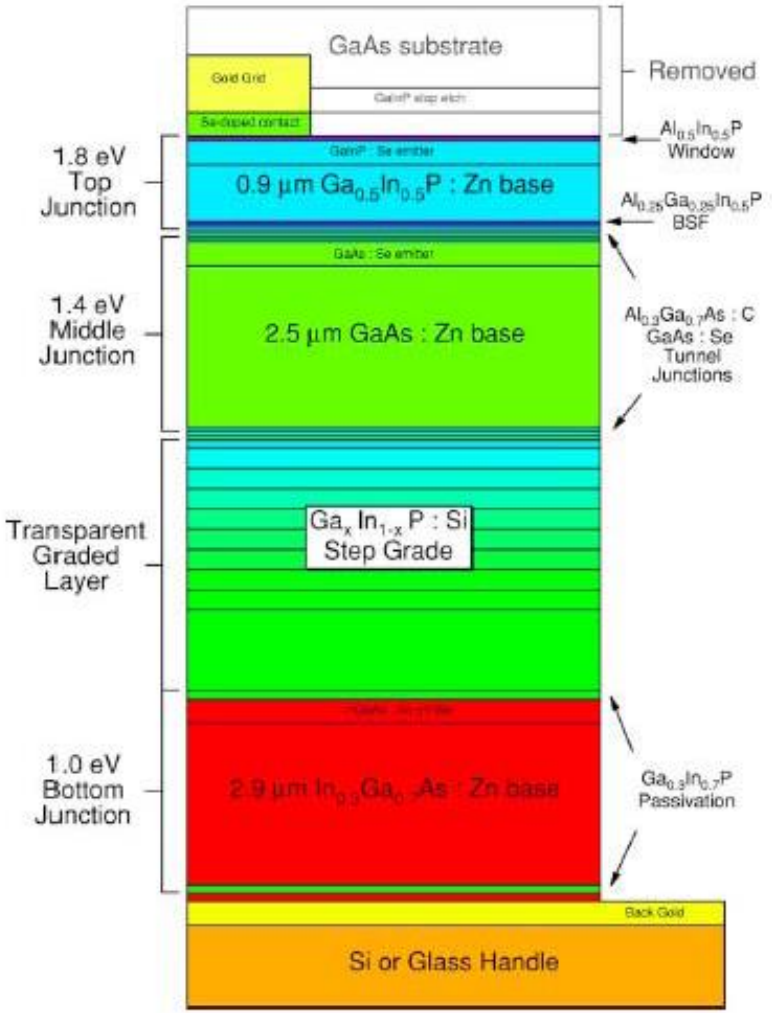
Monolithic materials integration is required for many future applications – as well as platforms for interesting science

- Multi-junction solar cells
- Optic components integrated into Si circuits
- Sensors with readout and transmission capability
- New multi-functional materials



Geisz *et al.*, APL **91**, 023502 (2007)

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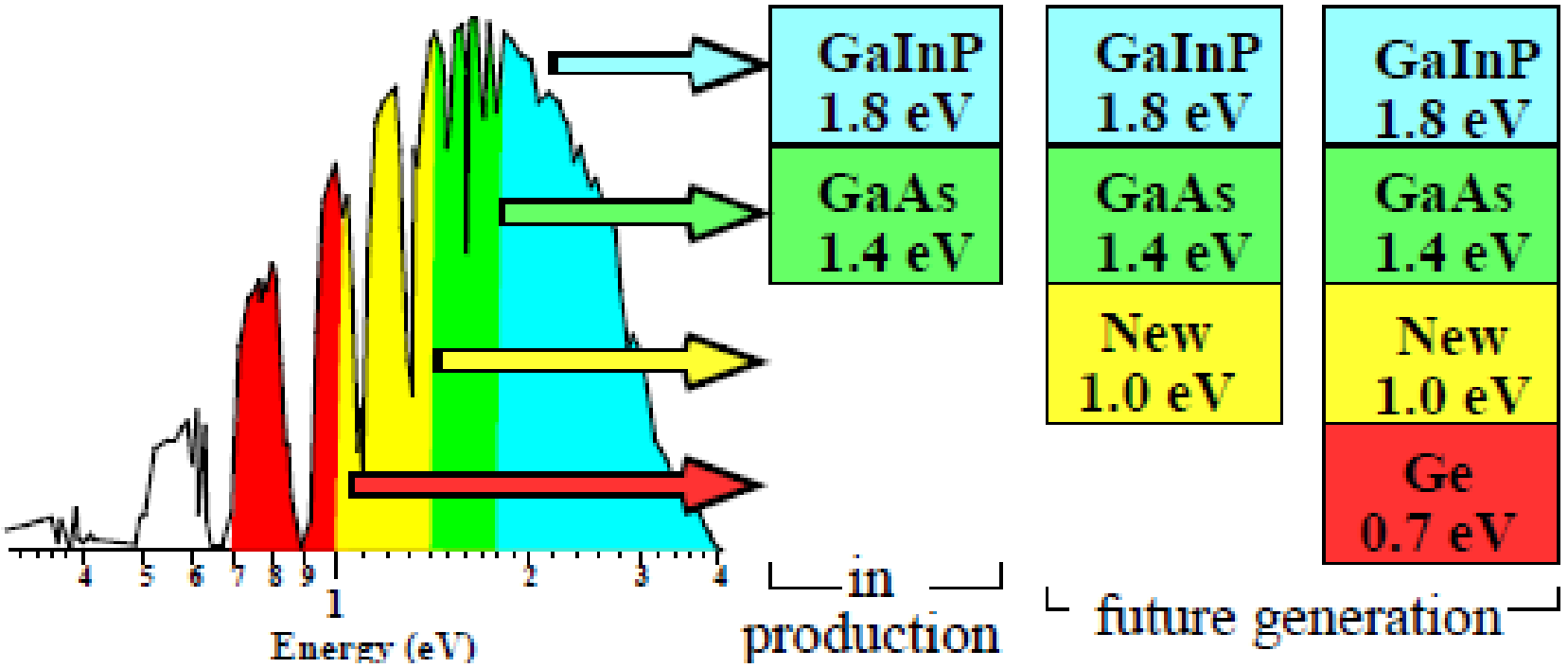
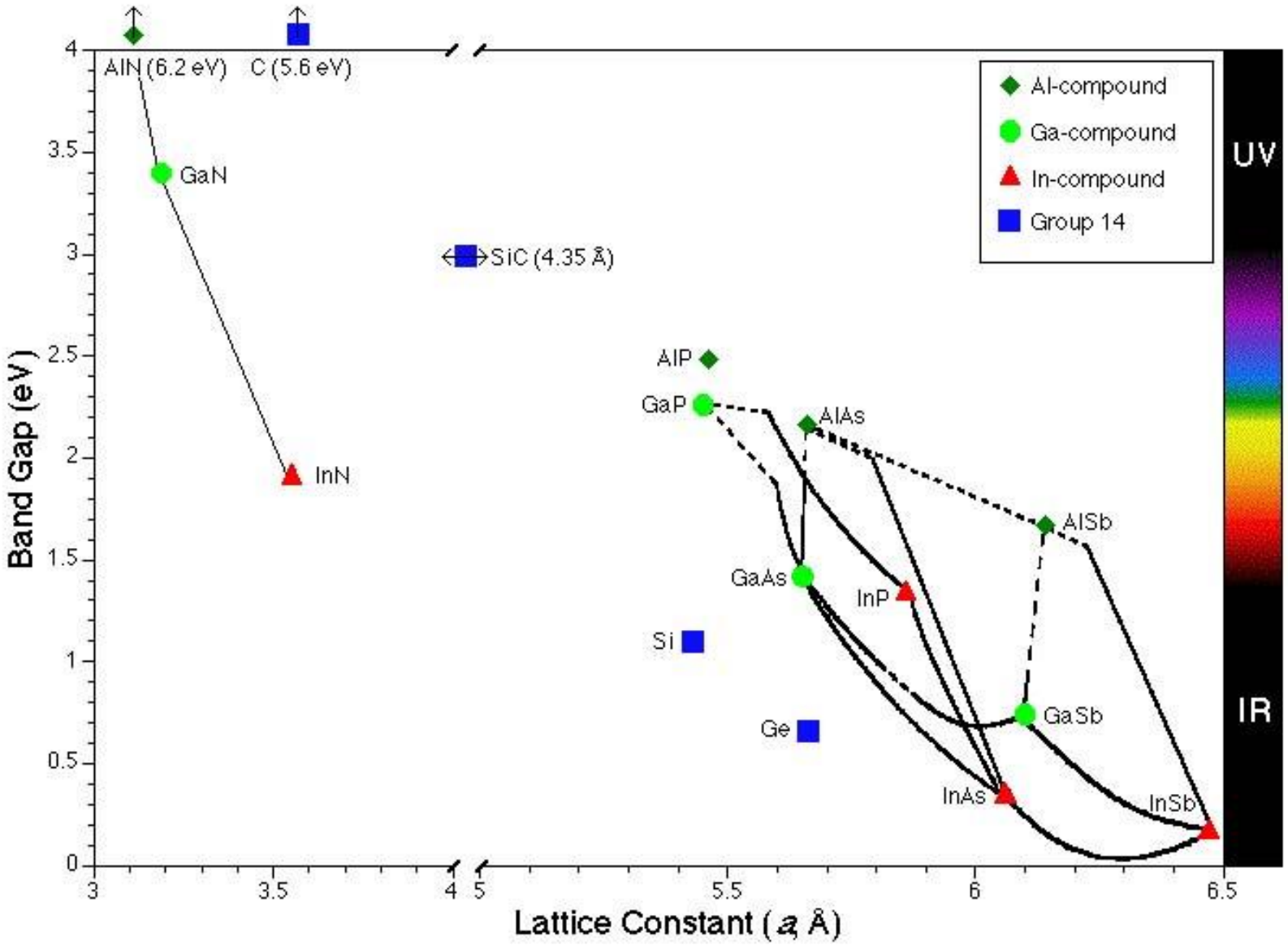
Multi-junction Solar Cells

Calculated Efficiencies (Ideal)			
500X, AM1.5D:	36%	47%	52%
1-sun, AM0:	31%	38%	41%

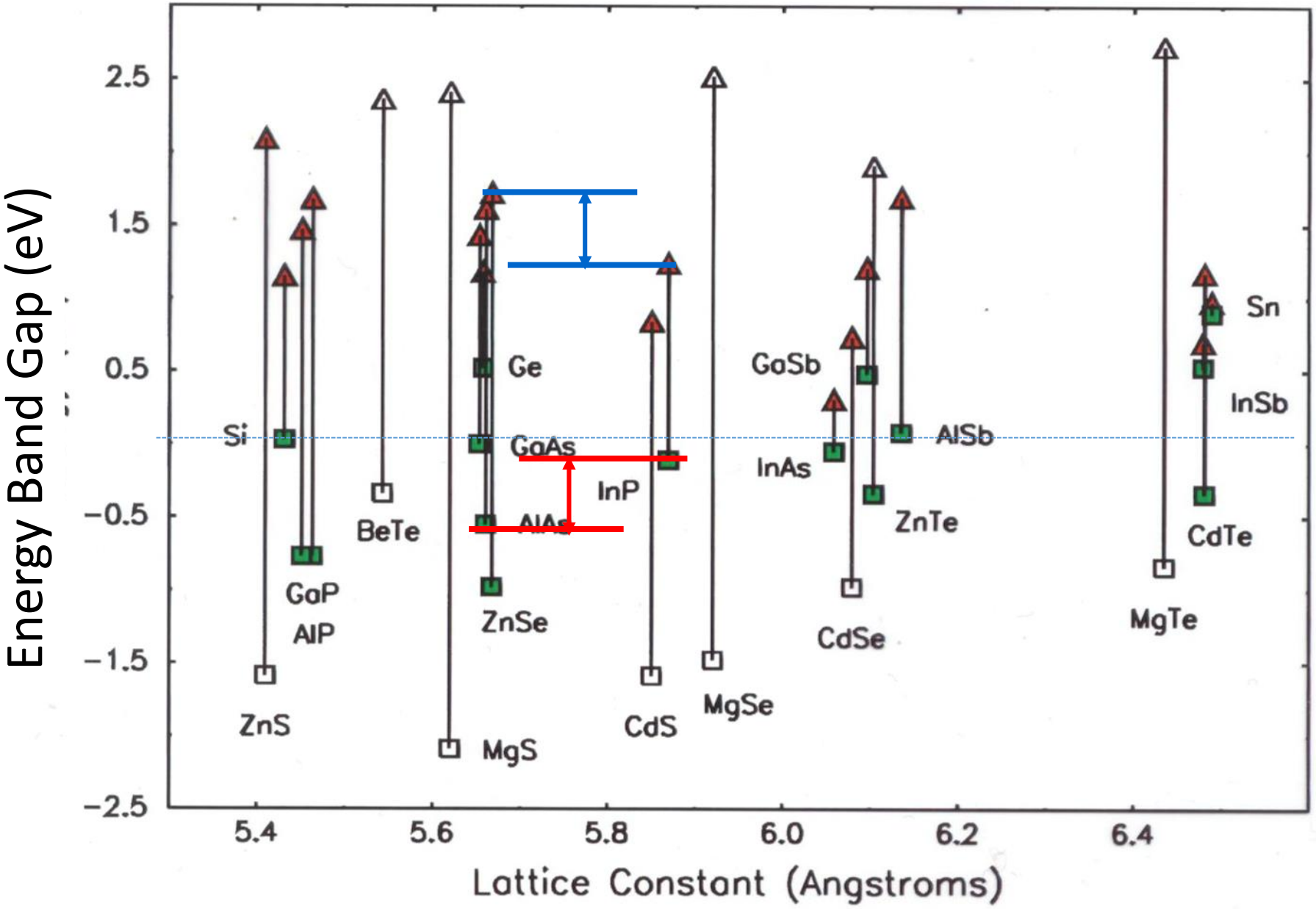


http://www.osti.gov/bridge/servlets/purl/6603-iNrNNH/webviewable/6603.pdf


AlN (6.2 eV)
C (5.6 eV)
GaN
SiC (4.35 Å)
InN
AlP
GaP
AlAs
AlSb
GaAs
InP
Si
Ge
GaSb
InAs
InSb
Al-compound
Ga-compound
In-compound
Group 14
UV
IR
Band Gap (eV)
Lattice Constant (a, Å)
0
0.5
1
1.5
2
2.5
3
3.5
4
3
3.5
4
5
5.5
6
6.5

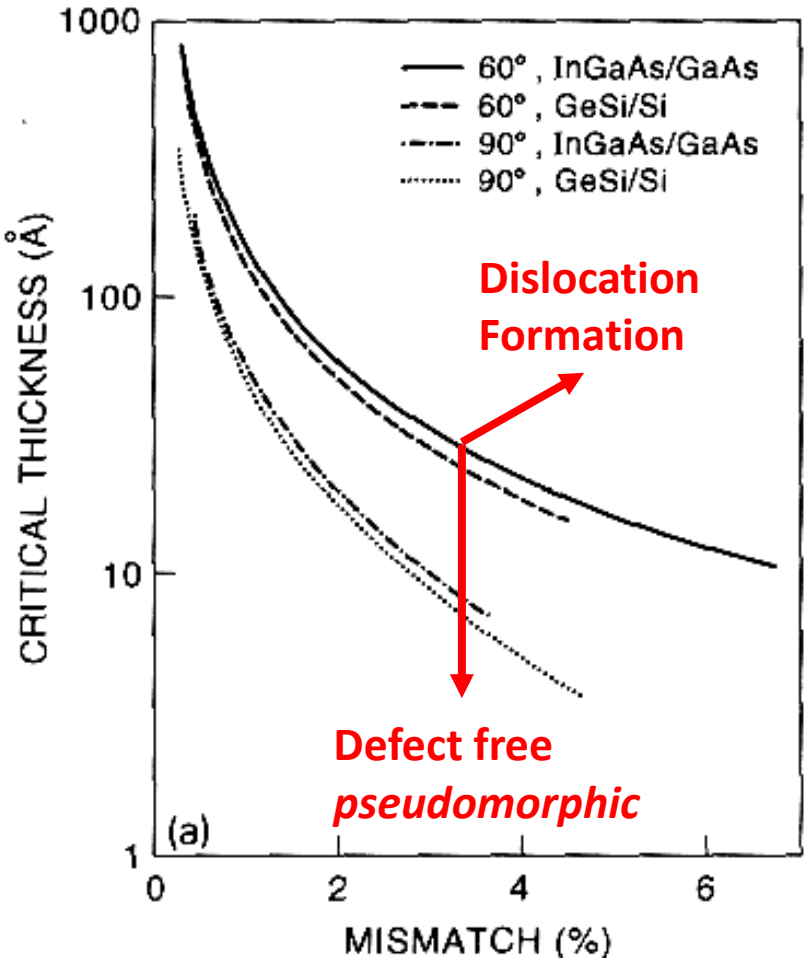
$$\Delta E_C = E_C^{InP} - E_C^{AlAs}$$

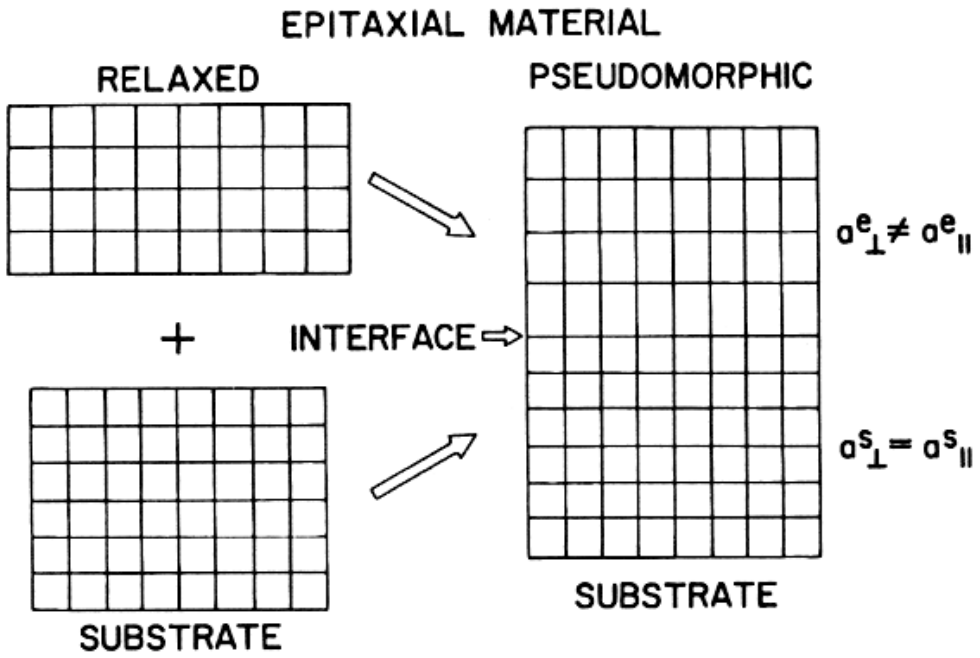
$$\Delta E_v = E_v^{InP} - E_v^{AlAs}$$



Limits to Pseudomorphic Growth

strain limits growth of pseudomorphic film on thick substrate





'Matthews-Blakeslee' model

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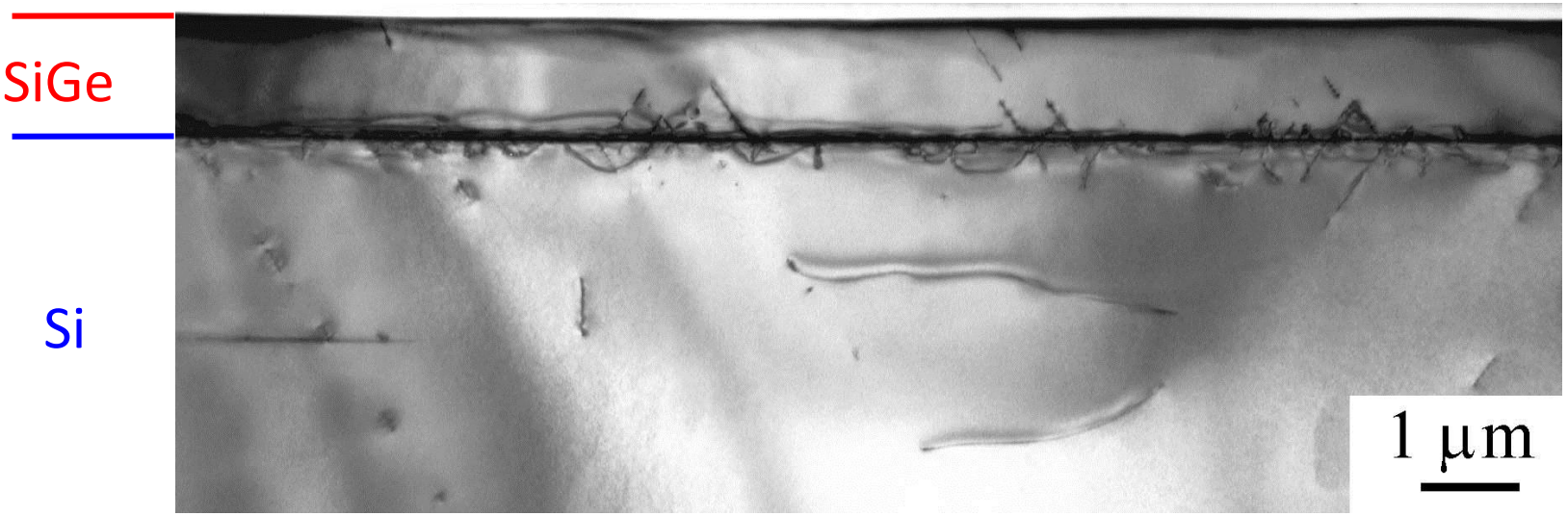
Substrate Dislocations in Bulk Si

XTEM of relaxed SiGe on bulk Si



- Large dislocation loops in the substrate.
- Routinely observed in SiGe/Si and InGaAs/GaAs
- Caused by dislocation-dislocation interactions

Micrograph by T.S. Kuan – SUNY Albany

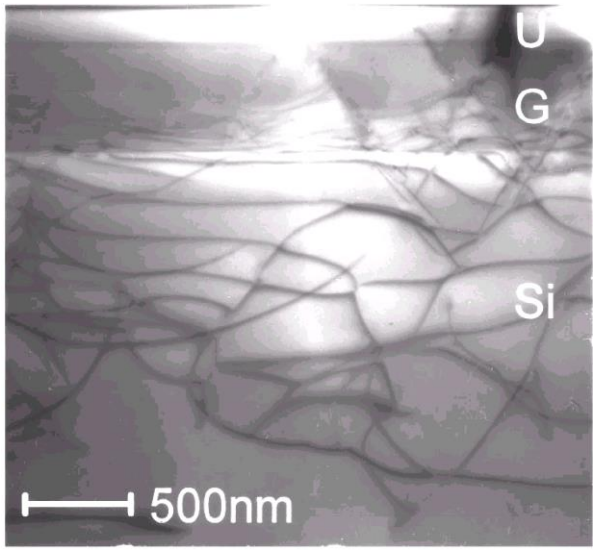
Materials Integration

Lots of Known Approaches:

- Buffer layers
  - Strained layer superlattices
  - 'thick' - Metamorphic buffers
- Wafer bonding/Layer transfer
- Structured substrates
  - Lateral epitaxial overgrowth – grow over masked regions
  - Nanopatterning

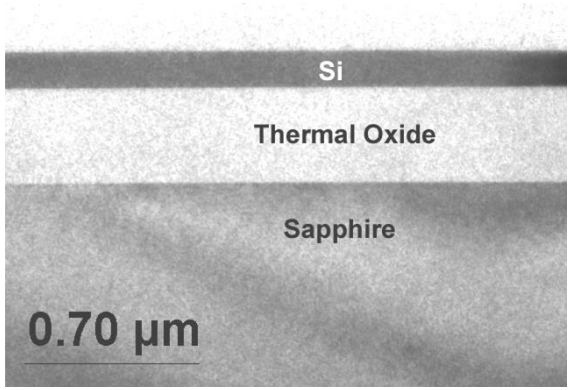
Methods to Integrate Lattice-mismatched Materials

Metamorphic Buffers: Growth on a Compositionally-Graded Layer



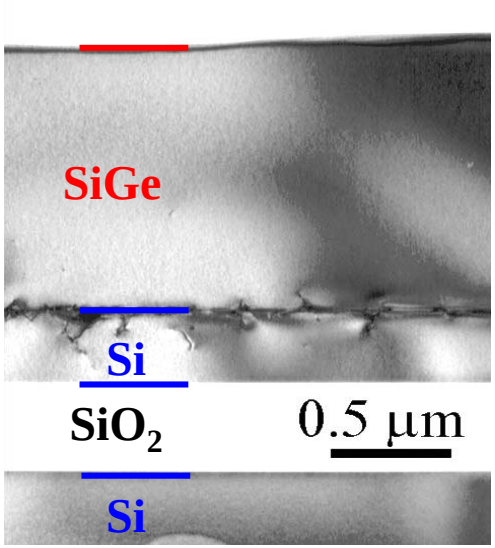
Hammond et al, Appl. Phys. Lett. **71**, 2517 (1997).

Bonding of Strain-relaxed Layers



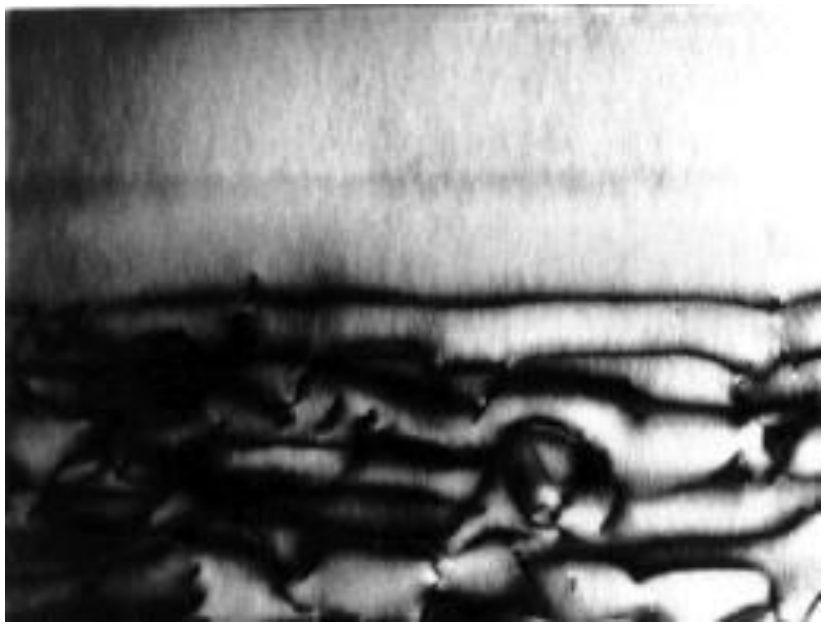
SOI: Silicon on Insulator

Growth on structured substrates



Metamorphic transition regions

n^{++}-$In_{0.53}Ga_{0.47}As$ contact	: 20nm
InP etch stop	: 6nm
$In_{0.52}Al_{0.48}As$ top barrier	: 8nm
Si delta-doped layer	
$In_{0.52}Al_{0.48}As$ spacer layer	: 5nm
$In_{0.7}Ga_{0.3}As$ channel	: 13nm
$In_{0.52}Al_{0.48}As$ bottom barrier	: 100nm
$In_xAl_{1-x}As$ graded buffer (x=0-0.52)	: 0.7-1.1μm
GaAs nucleation and buffer layer	: 0.5-2.0μm
4°(100) Off-cut p-type Si substrate	



Metamorphic Buffer

http://www.electroiq.com

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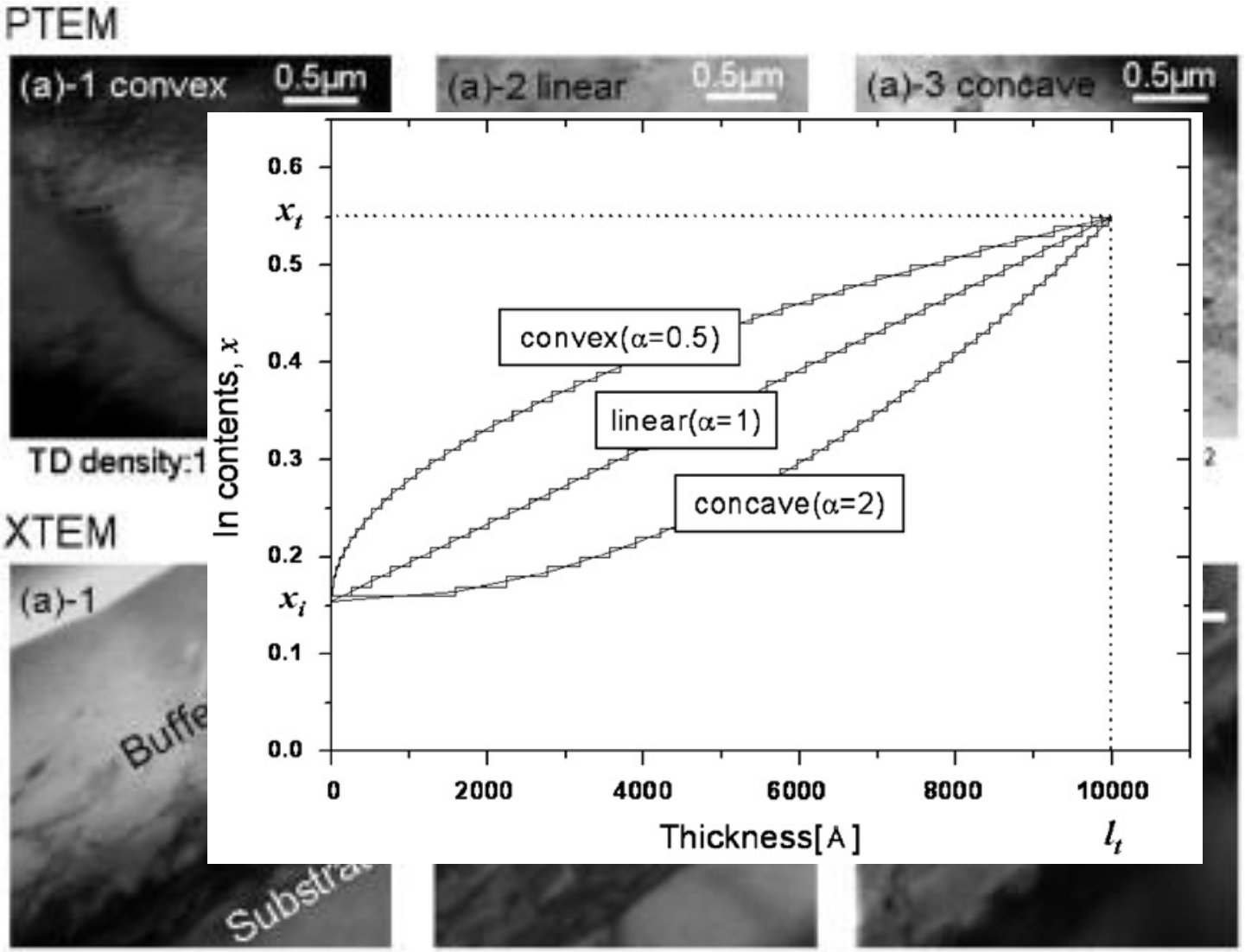
Metamorphic Buffer Layers



$$\frac{dD}{dx} = -k_1 D - k_2 D^2$$

Compositionally graded layers

- MBE
- MOVPE
- HVPE

Choi et al, JCG 311 (2009) 1091

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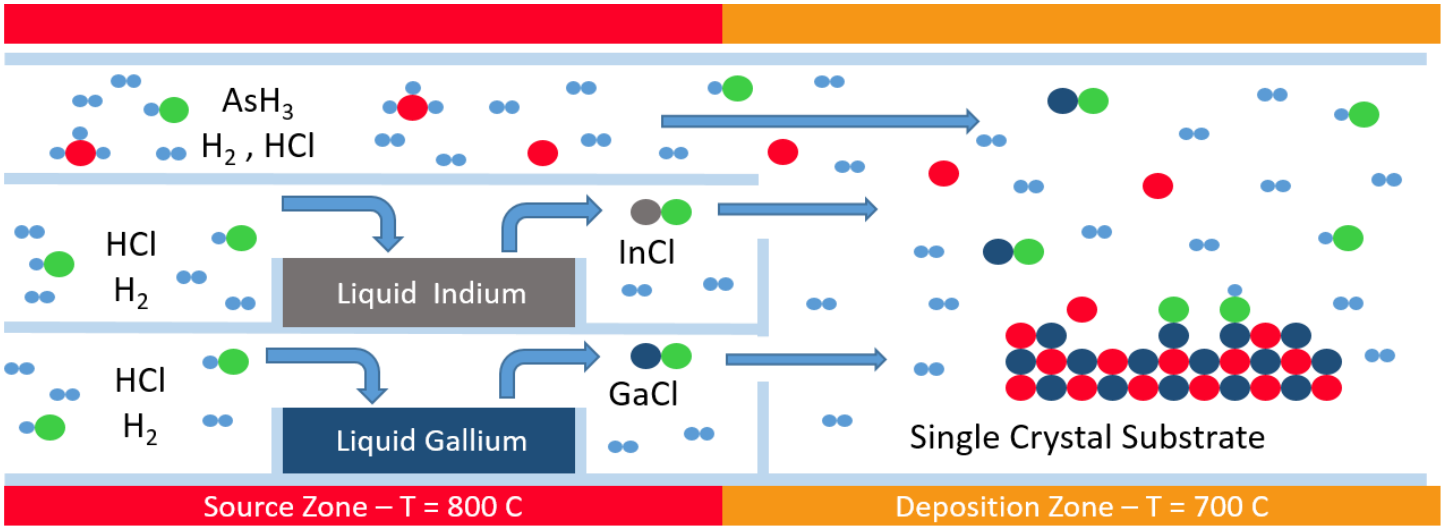
The HVPE Process: Growth of Metamorphic buffers



- Hydride HVPE – Ga(In)Cl generated by passing HCl over Ga(In) source; group V atom enters as hydride (AsH_3)
- V-III ratio variable in Hydride process
- Near-equilibrium process

$$Ga + HCl \Rightarrow GaCl + \frac{1}{2}H_2$$

$$GaCl + \frac{1}{2}As_2 + \frac{1}{2}H_2 \Leftrightarrow GaAs + HCl$$

$$AsH_3 \Rightarrow \frac{y}{2}As_2 + \frac{1-y}{4}As_4 + \frac{1}{2}H_2$$

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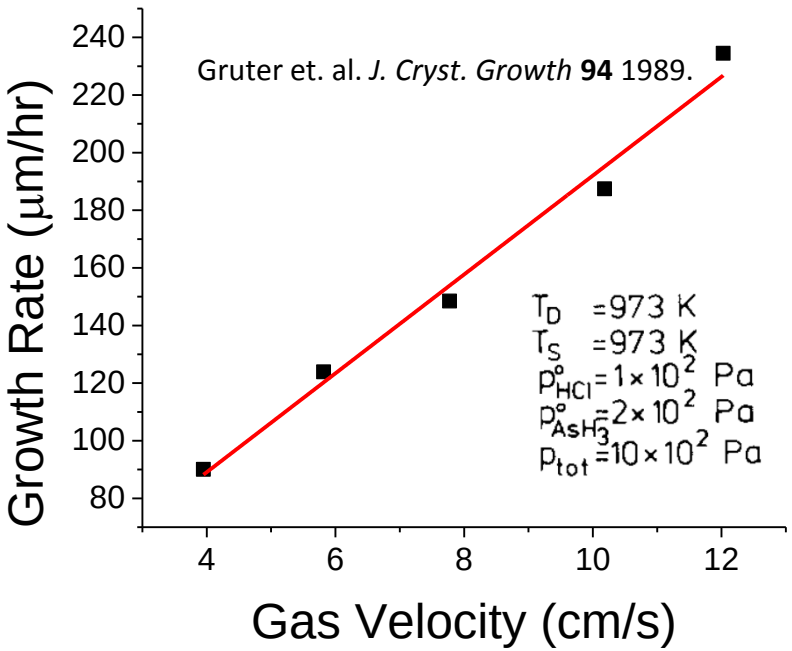
MOVPE vs HVPE



- High growth rates
- Lower cost group III precursor
- Low V:III ratios

	HVPE	MOVPE
Growth Rate (µm/hr)	1-300 (low pressure)	1-20
Bulk Ga cost ($/g)	0.80	5
V:III	2-3	30-80

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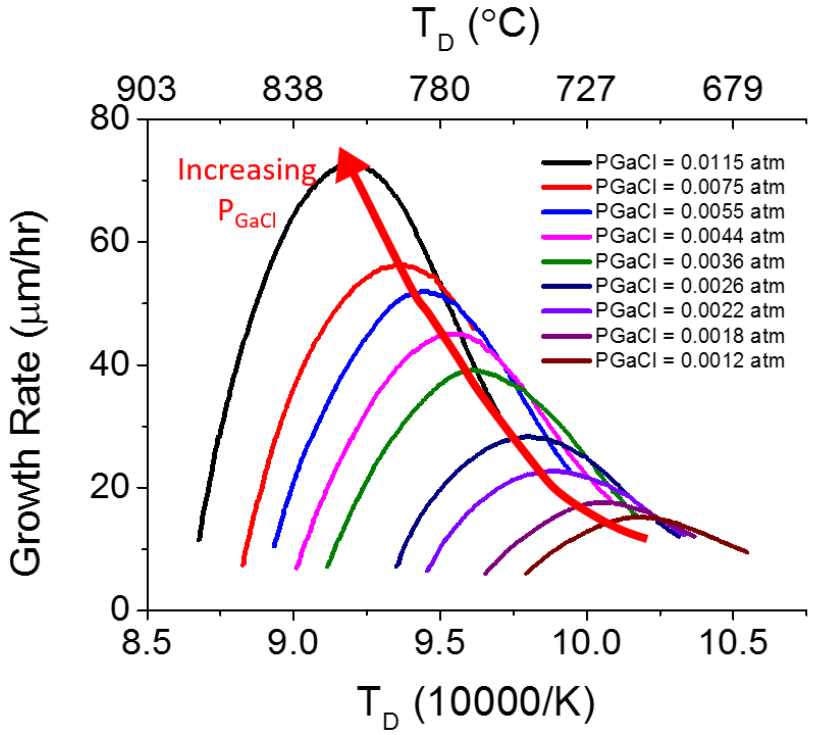
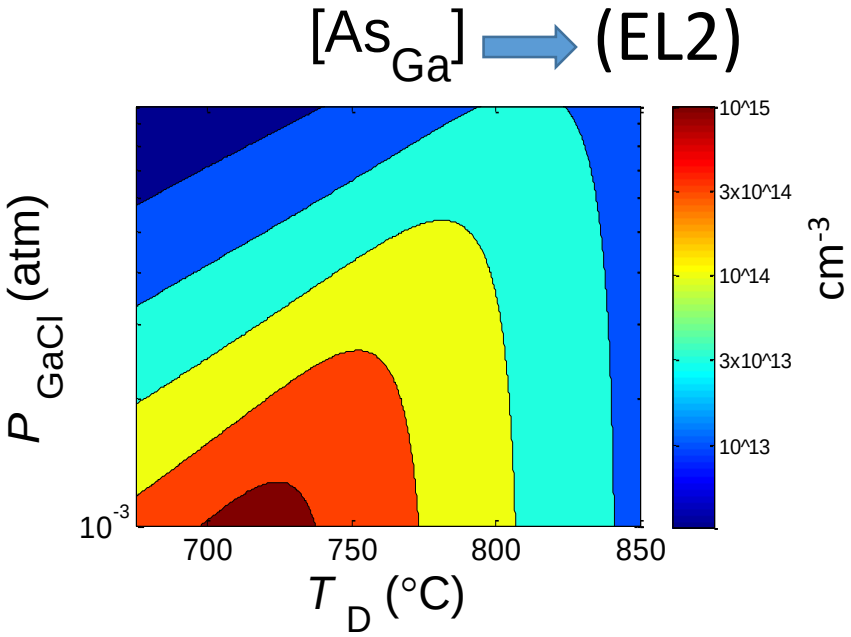
Implications for Growth





Shaw, D.W. *J. Electrochem. Soc.* **117** (1970)

- The maximum in growth rate occurs at higher temperatures as P_{GaCl} is increased
- The equilibrium level of EL2 decreases with T_D ->desirable to operate at high P_{GaCl} and T_D

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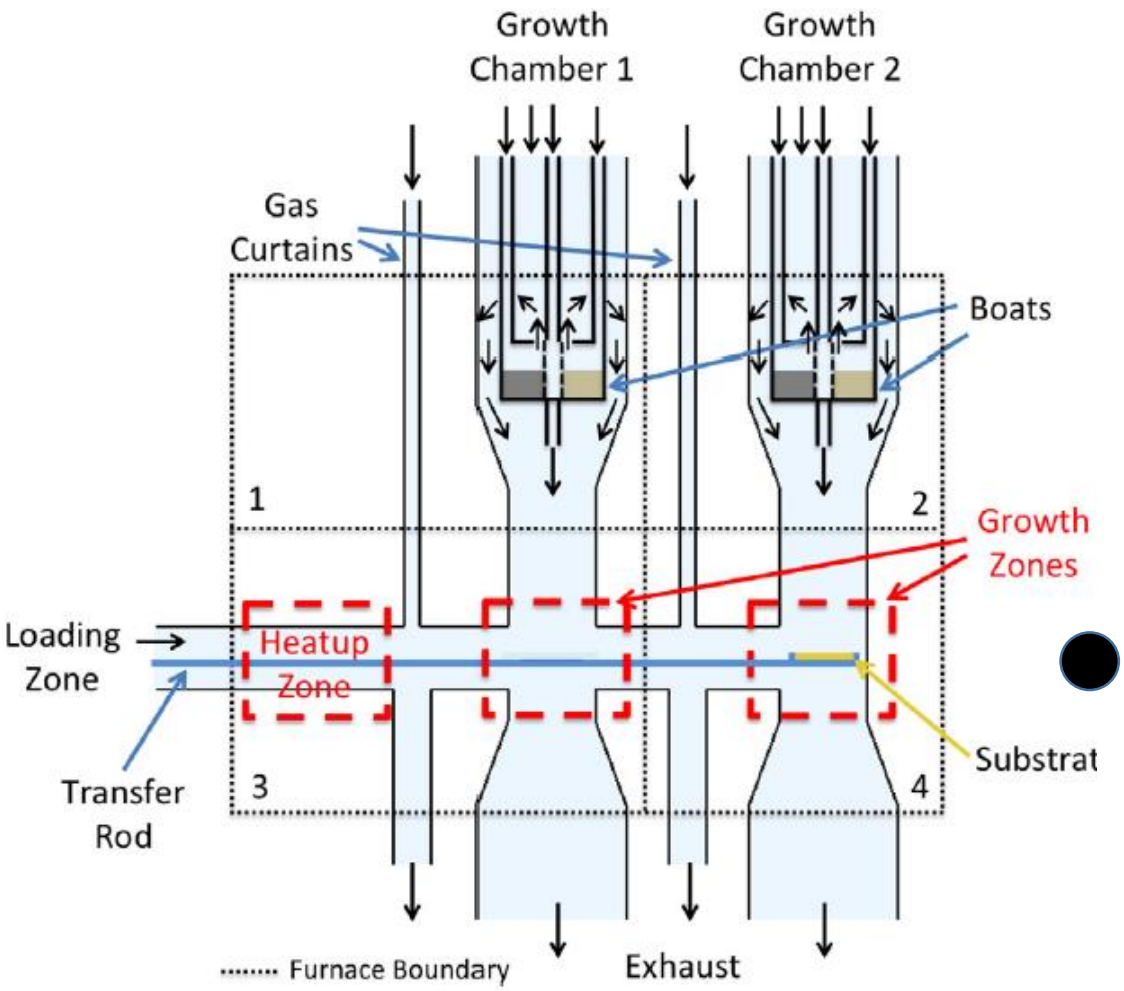
Base Region Emitter Region



Design for a high throughput HVPE system: Serial chambers for layered growth

Kevin L. Schulte,et al. J. Crystal Growth 434 (2016) 138–147

Hydride Vapor Phase Epitaxy: New design for an open system

$GaCl$

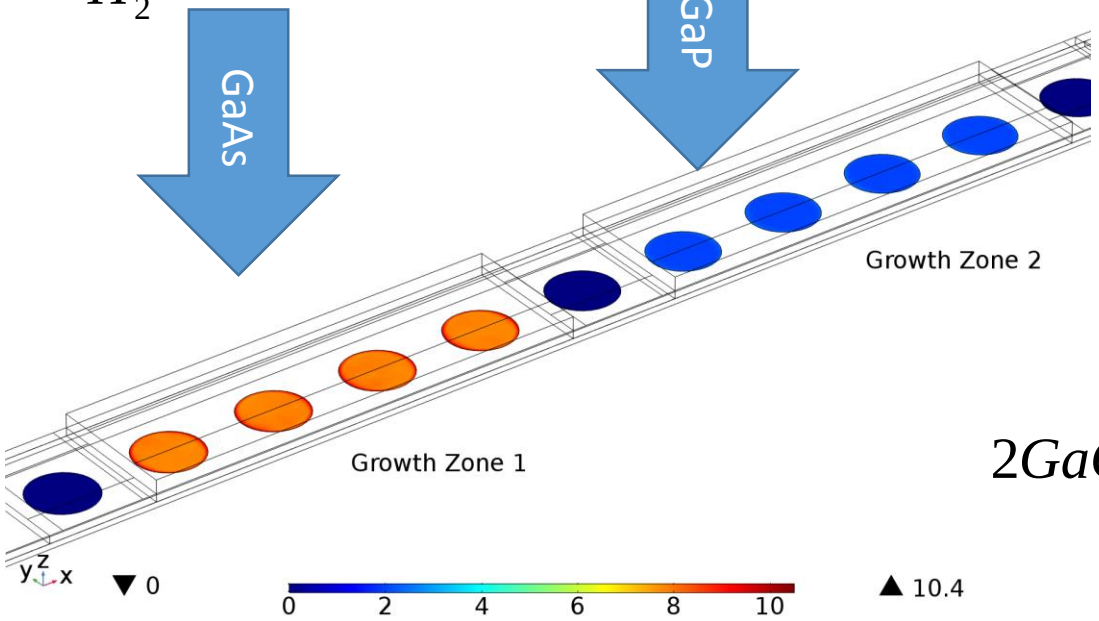
$As_2 - As_4$

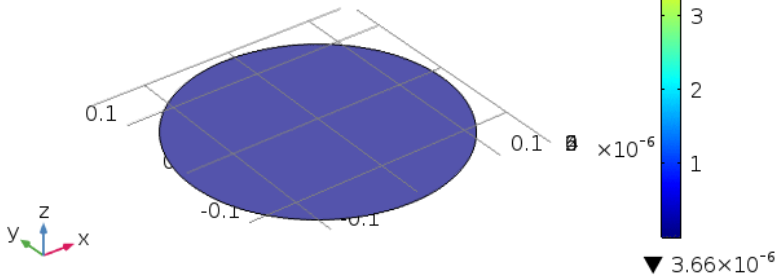
H_2

$GaCl, InCl$

$P_2 - P_4$

H_2

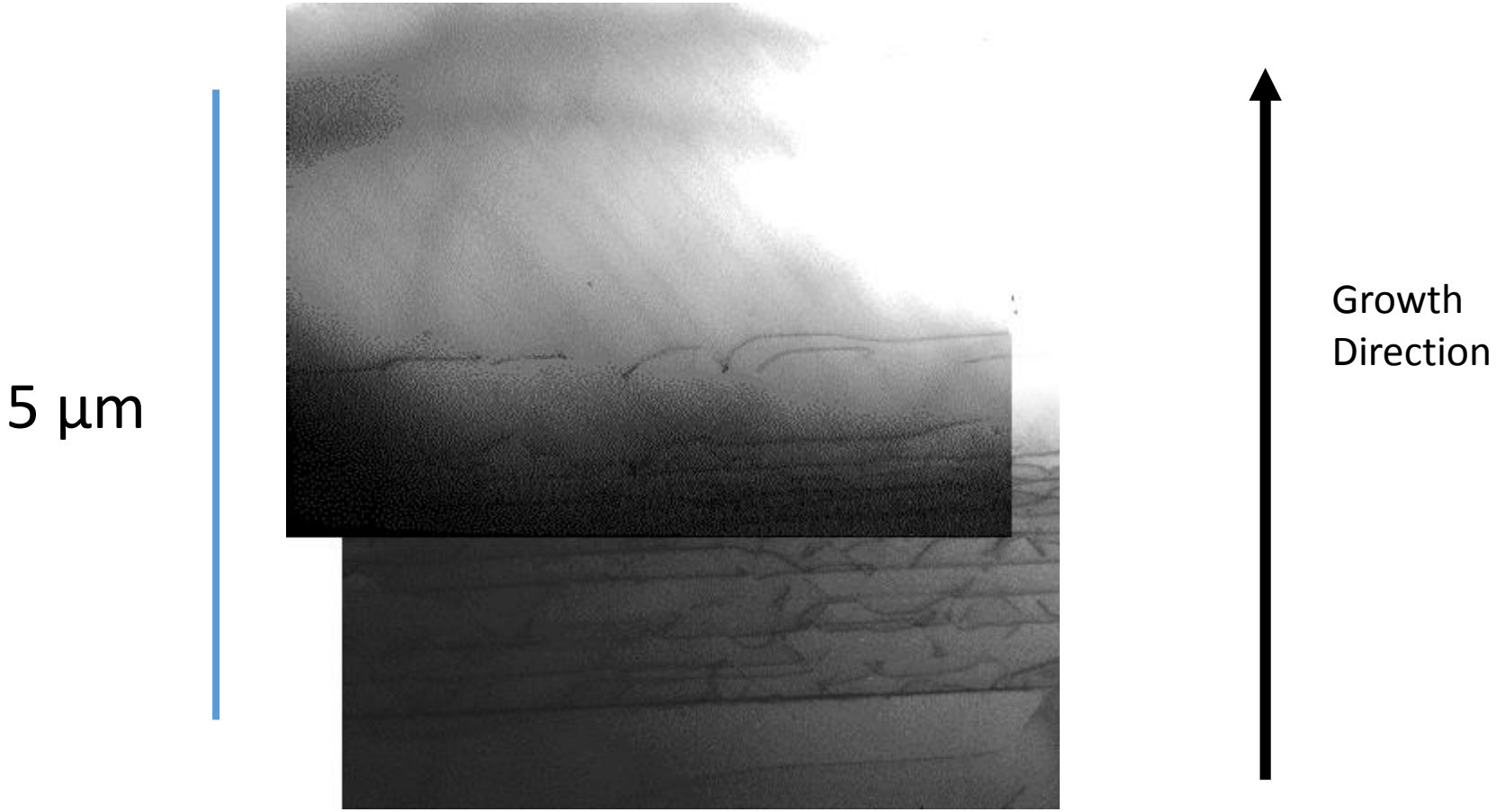




Integrated Growth Models to predict process results

$$2GaCl + As_2 + H_2 \Leftrightarrow 2GaAs + 2HCl$$

Yao, Rawlings, Kuech, unpublished



- Thickly capped samples exhibit dislocations *above* the final compositional interface
- These dislocations appear to be gliding upwards from below
- The capping layer exhibits multiple strain states

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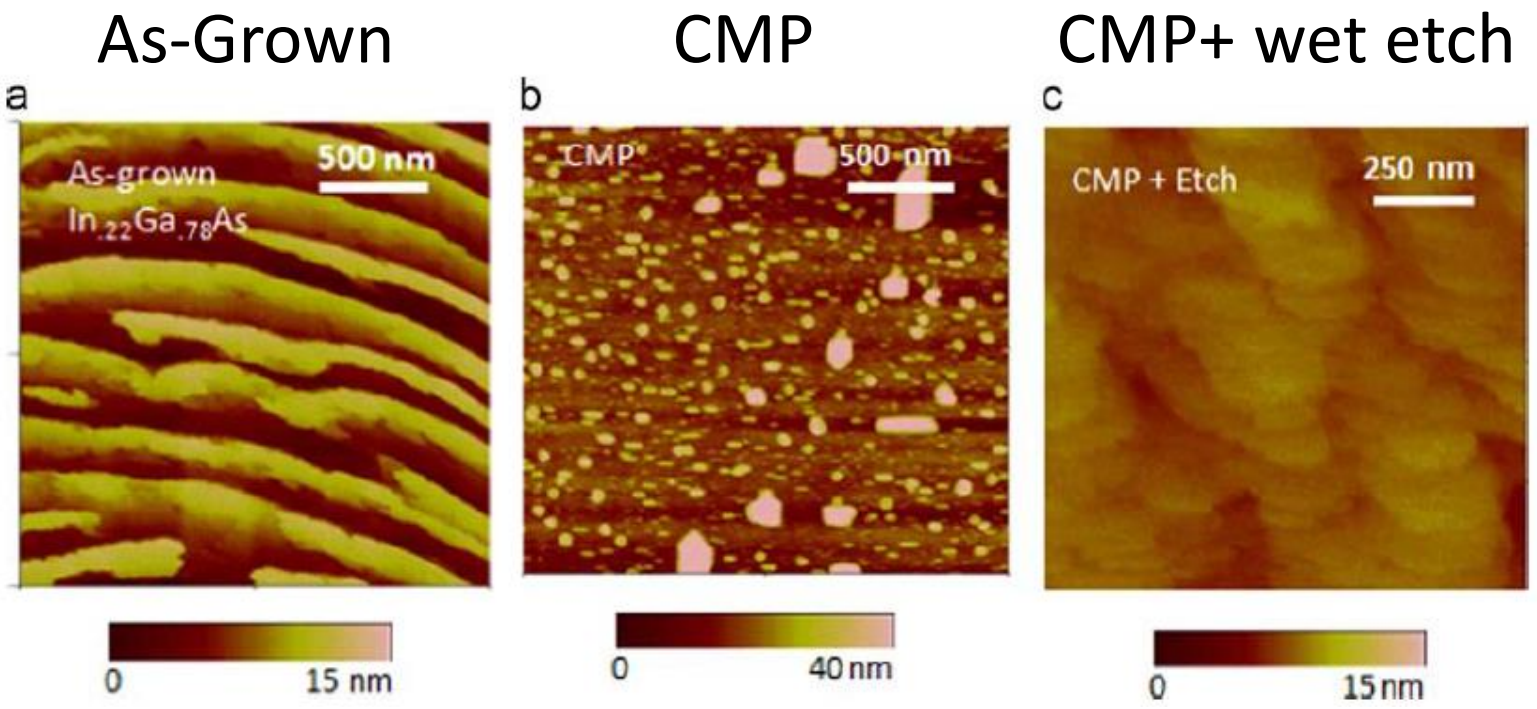
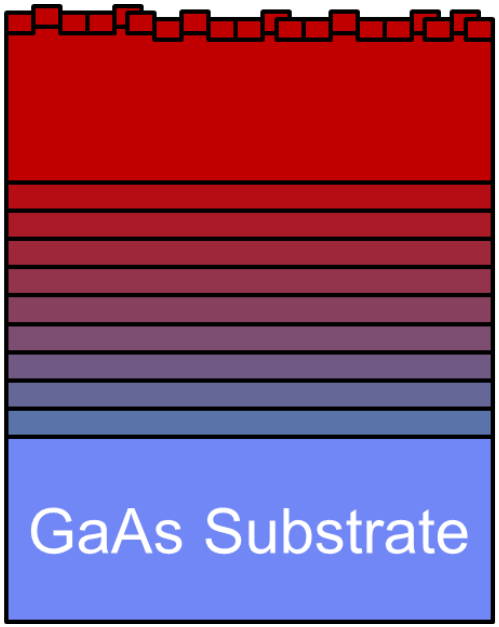
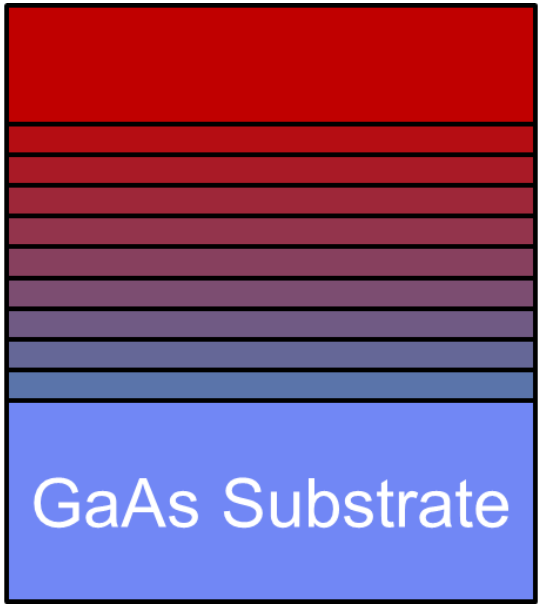
$In_{0.22}Ga_{0.78}As$ on Grade buffer on a GaAs

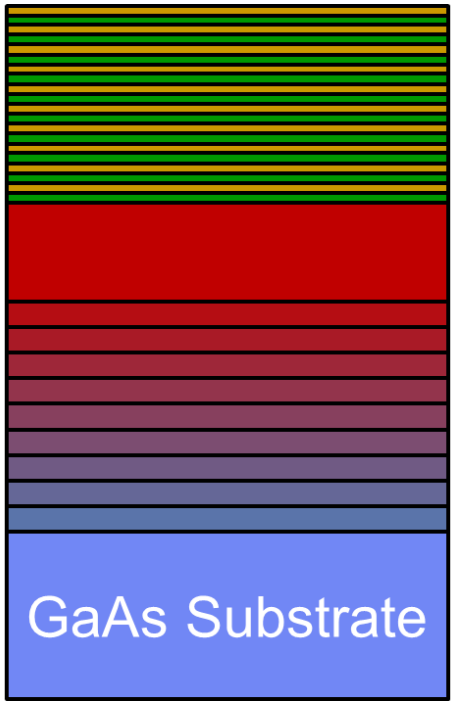


8 µm Cap

Process Flow







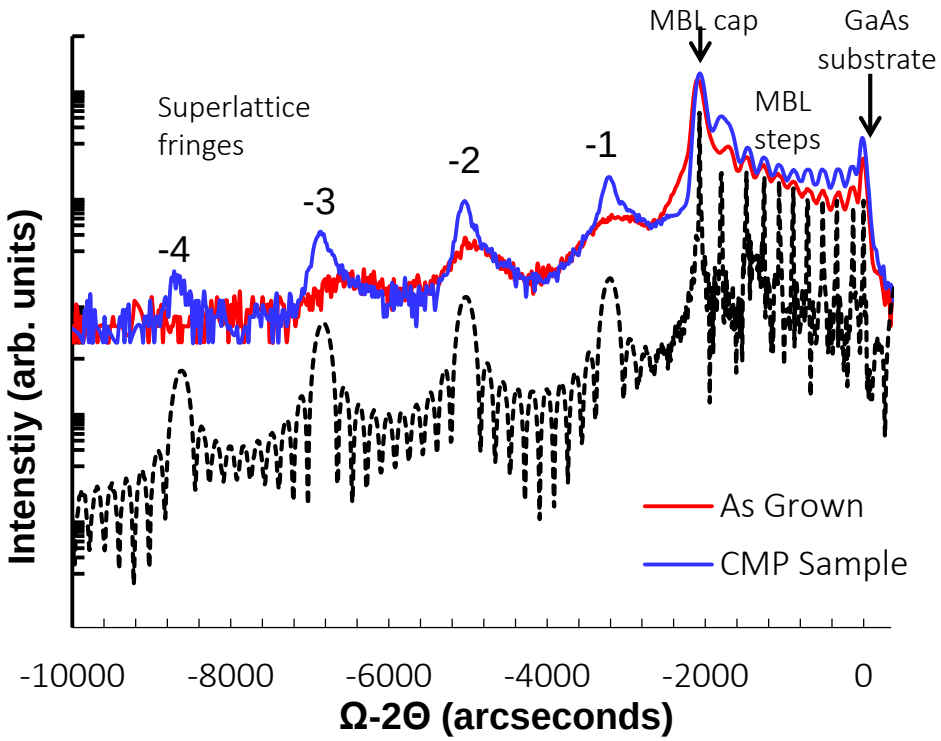
Surface rough after HVPE growth of MBL devices

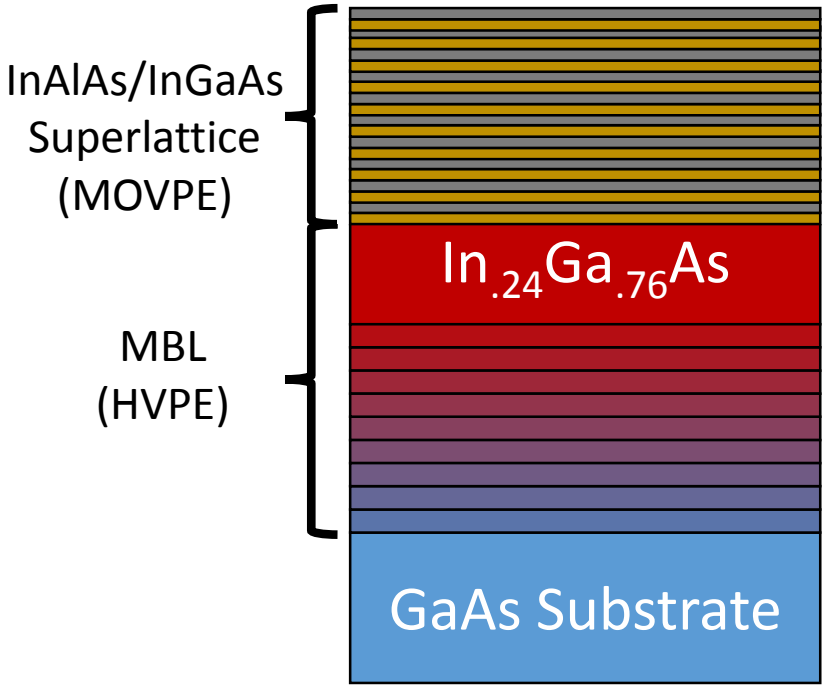
- Planarization by CMP
- Ozone treatment
- Ammonium Hydroxide wet etch

Device structure grown on MBL substrate

HVPE Research at UW

Thick Metamorphic Buffer Layers (MBLs)





1. K.L. Schulte et al., *J. Cryst. Growth* **370**, 293-298 (2013).
2. L.J. Mawst et al., *IET Optoelectron.* **8**, 25-32 (2014).

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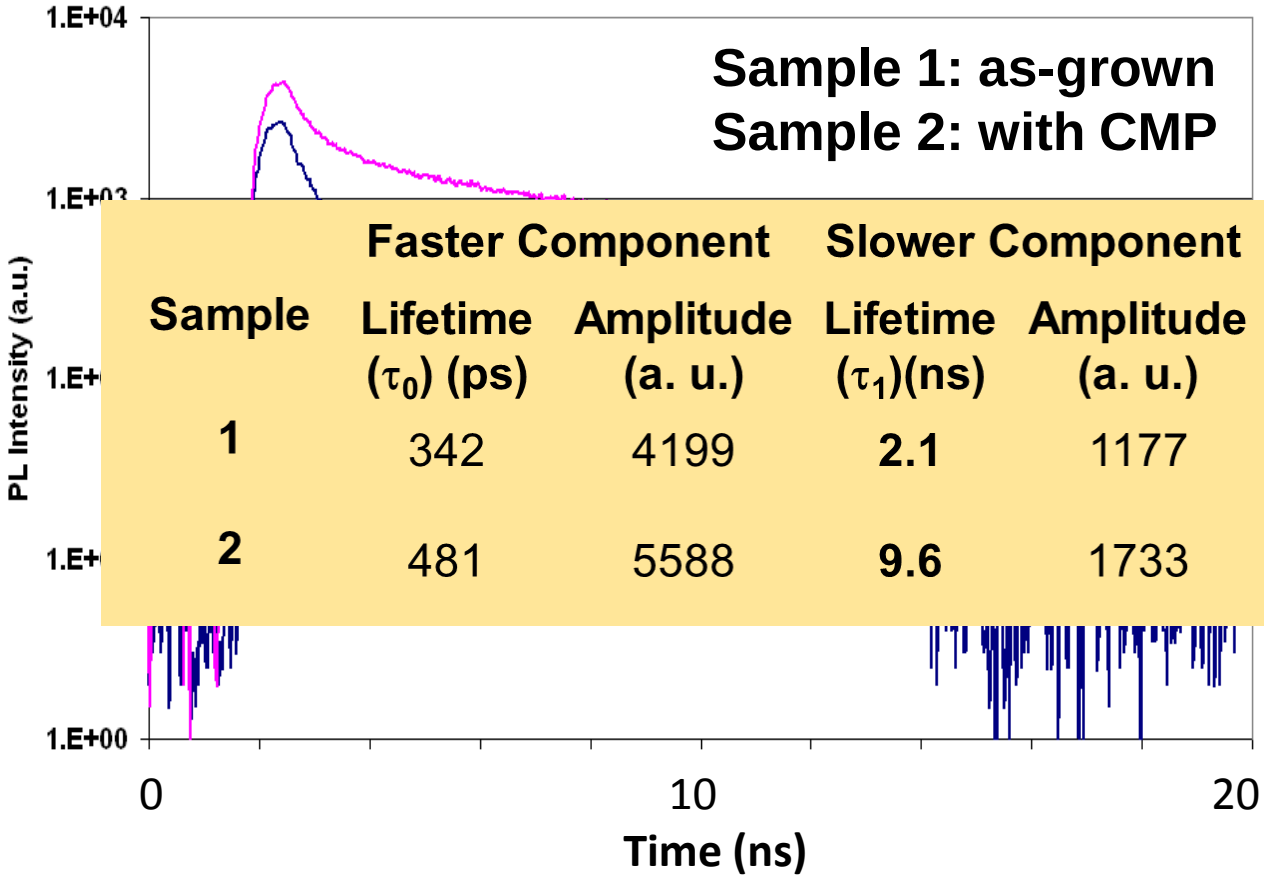
TR-PL Characterization of Bulk $In_{0.28}Ga_{0.72}As$ on MBL



Sample	Faster Component		Slower Component	
	Lifetime (τ_0) (ps)	Amplitude (a. u.)	Lifetime (τ_1)(ns)	Amplitude (a. u.)
1	342	4199	**2.1**	1177
2	481	5588	**9.6**	1733

- **Mode-locked Ti:Sapphire laser**
- **pulse duration of 120 fsec with rep. rate of 200 kHz**
- **excitation λ = 800 streak camera (IRF) ~30 ps**

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Metamorphic Buffer Layers

- Dislocation control through controlled introduction
- Applicable to all growth system
- Thick MBLs can achieve the limiting dislocation densities of 10^5-10^6 cm^{-2}
- HVPE can be used to form ultra thick MBLs for CMP-based processing
- When used in tandem with other processing can be reusable substrate

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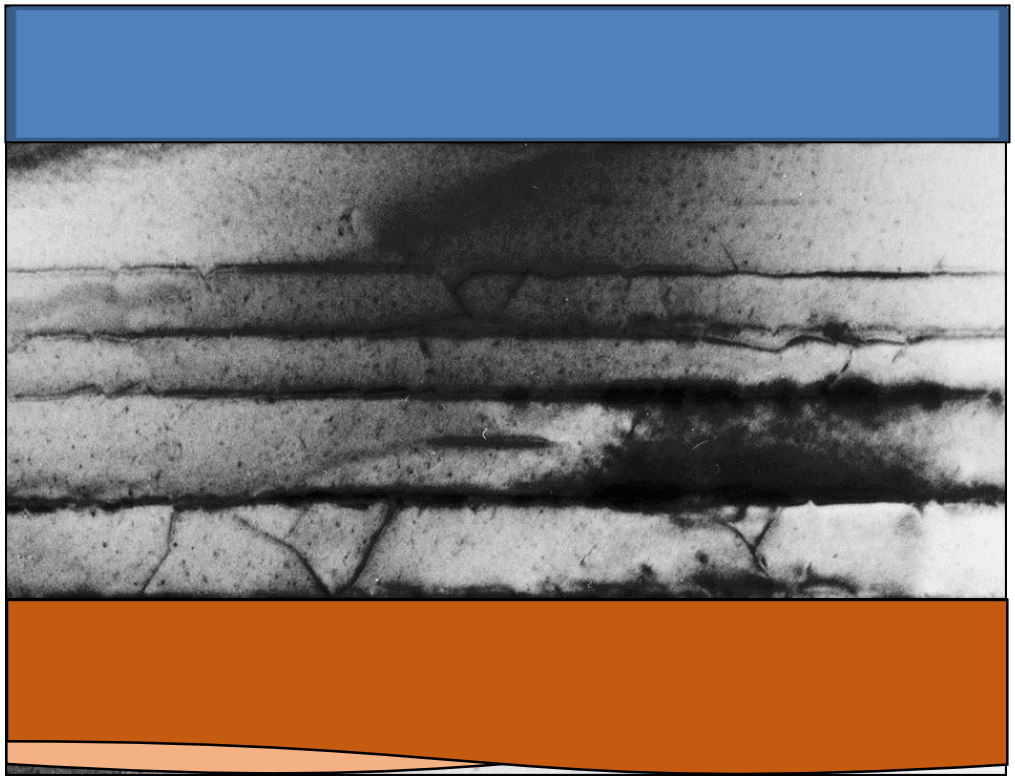
Alternative Substrates through layer transfer/wafer bonding

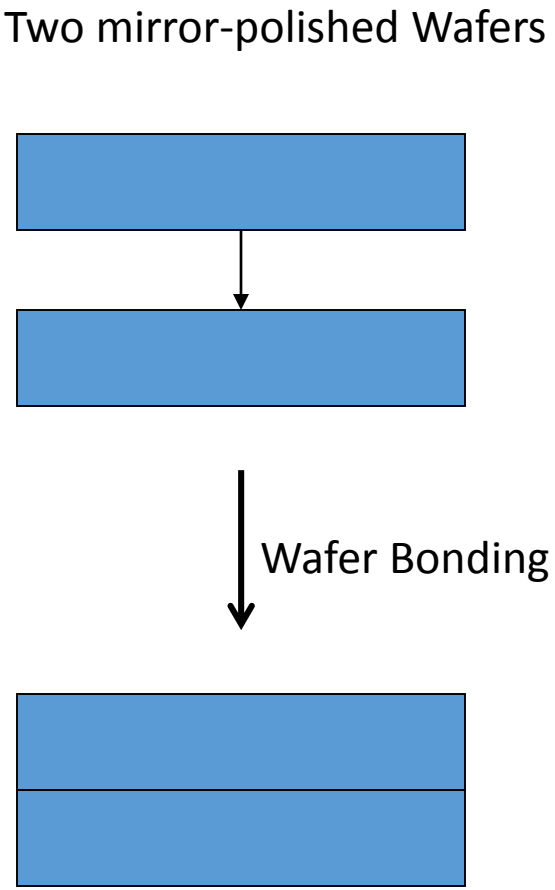
How to make the transition?



A Graded or Stepped Layer

Layer transfer/Wafer Bonding

Wafer Bonding Applications

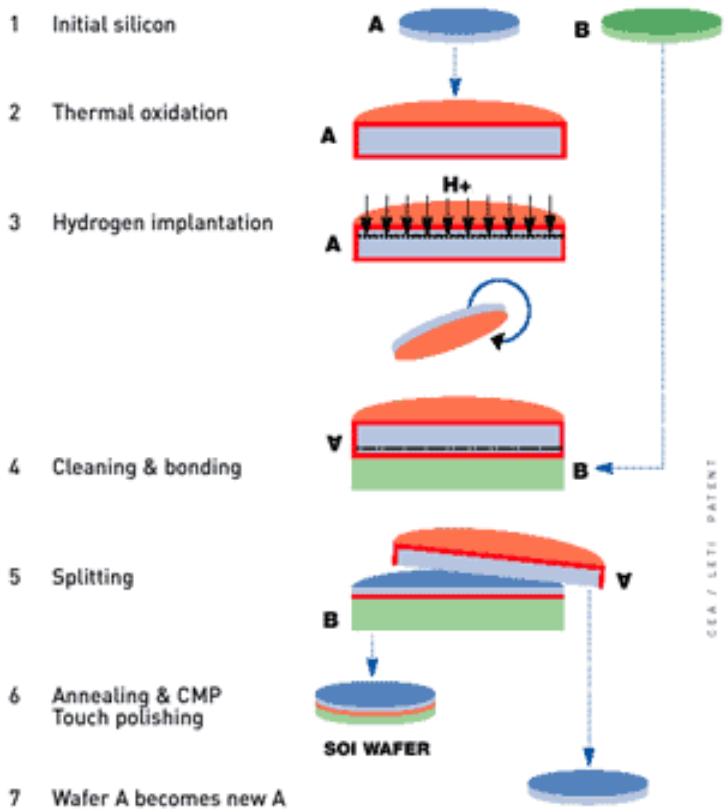


- Layer/device transfer
- Materials integration
- Substrate engineering

- Advantages:
  - Wafer-scale integration
  - Low temperature process
- Disadvantages:
  - Atomic smooth surface required
  - Voids formation at interface

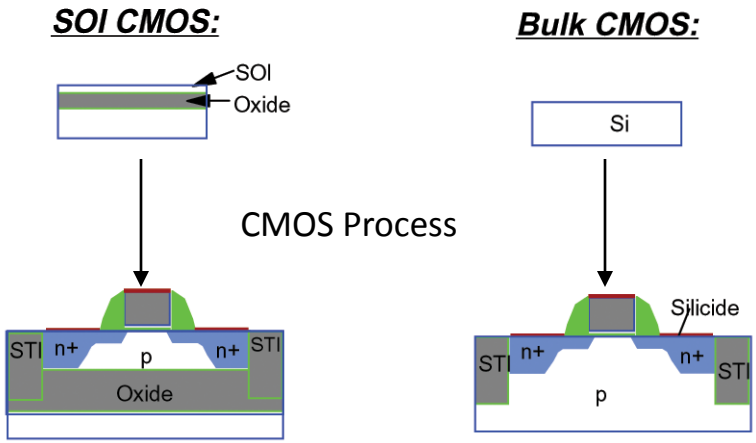
Wafer Bonding Applications: SOI

SOITEC's smart cut process to fabricate SOI wafers

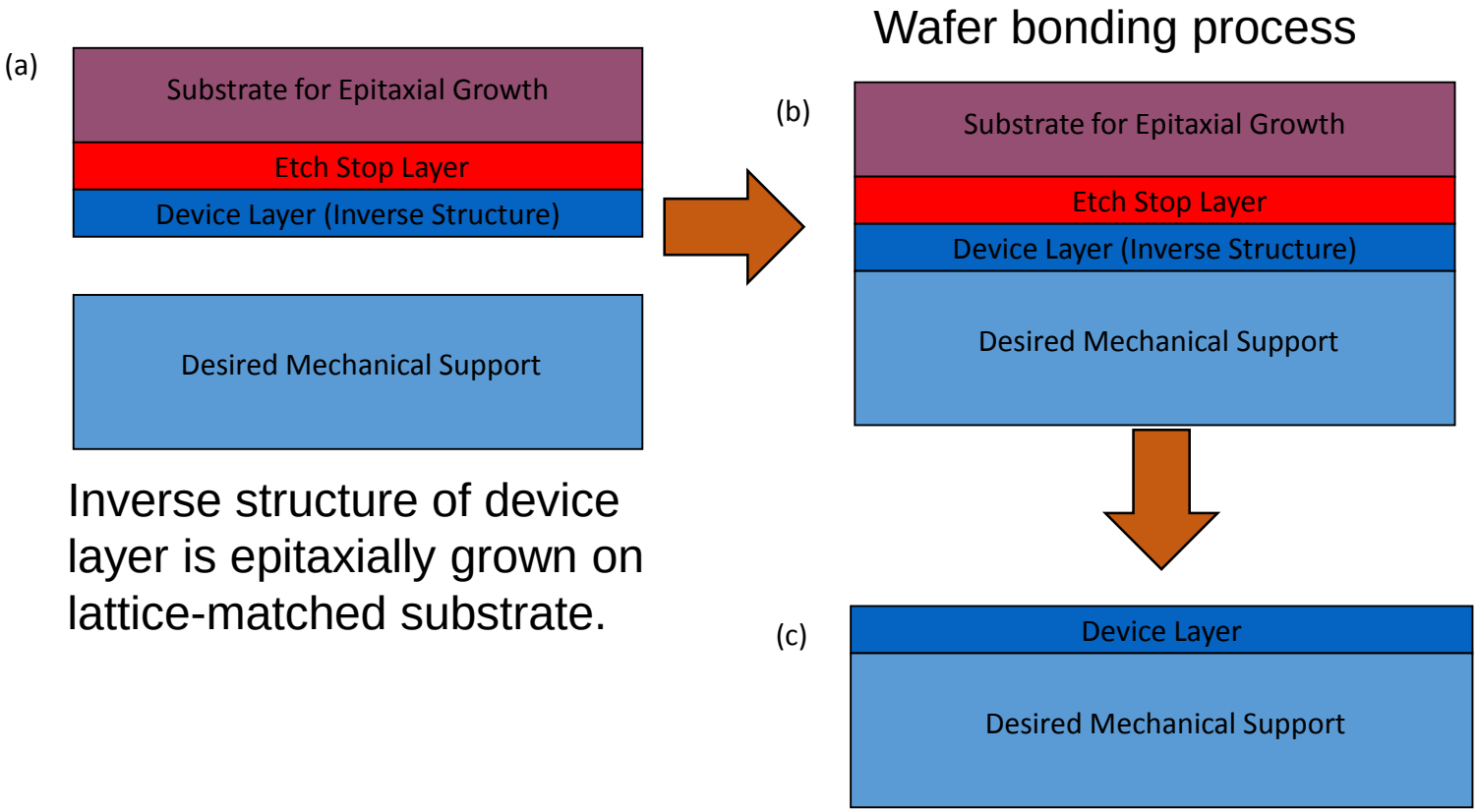


IBM's SOI CMOS will:

- Improve chip performance
- Reduce chip power



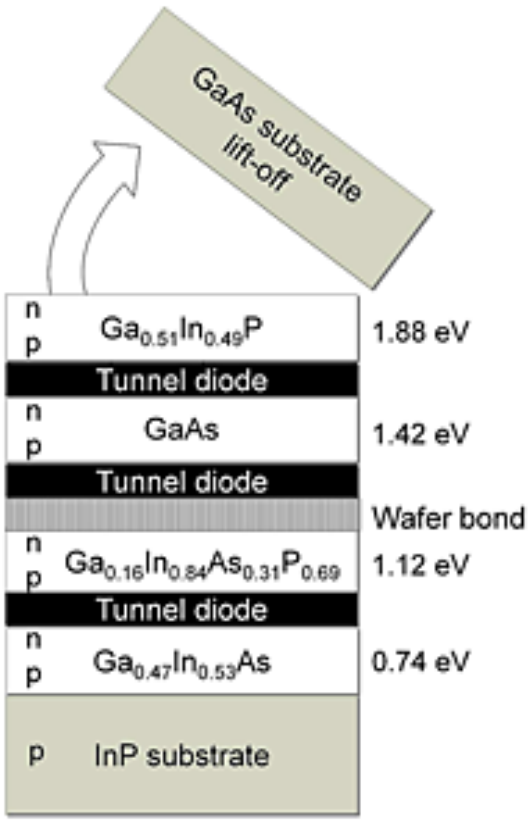
Layer Transfer Technique by Wafer Bonding



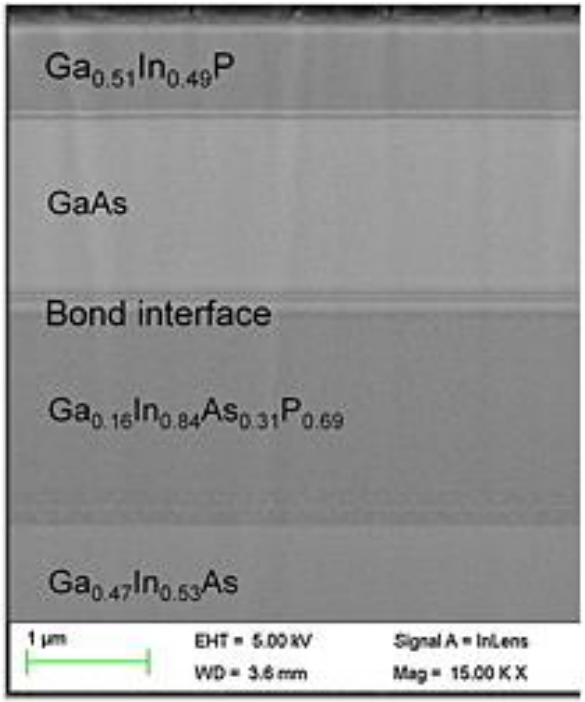
Inverse structure of device layer is epitaxially grown on lattice-matched substrate.

Mechanical lapping and selective chemical etching are used to remove the substrate for epitaxial growth, leaving the transferred device layer on the desired mechanical support.

Wafer Bonding Applications



Wafer bonded four-junction GaInP/GaAs//GaInAsP/GaInAs concentrator solar cells with 44.7% efficiency



Progress in Photovoltaics: Research and Applications
Volume 22, Issue 3, pages 277-282, 13 JAN 2014 DOI: 10.1002/pip.2475

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Requirements on Wafer-Wafer Bonding

Hydrophilic wafer bonding limitations are due to the macroscopically short-range van der Waal forces:

- Surface smoothness: RMS Roughness < 1 nm
- Surface flatness: Total Thickness Variation (TTV) < 10 µm
- Surface cleanliness: Hydrocarbons, water, metals
- Hydrophilic surfaces vs. hydrophobic

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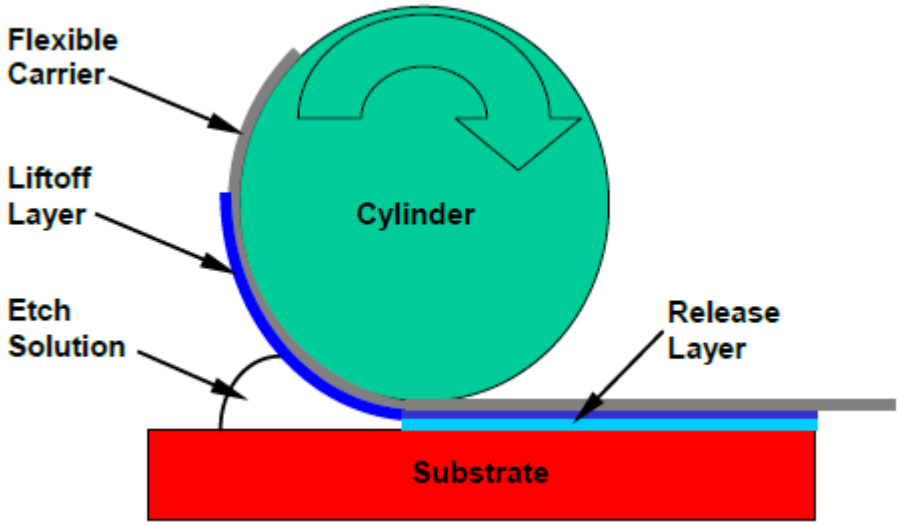
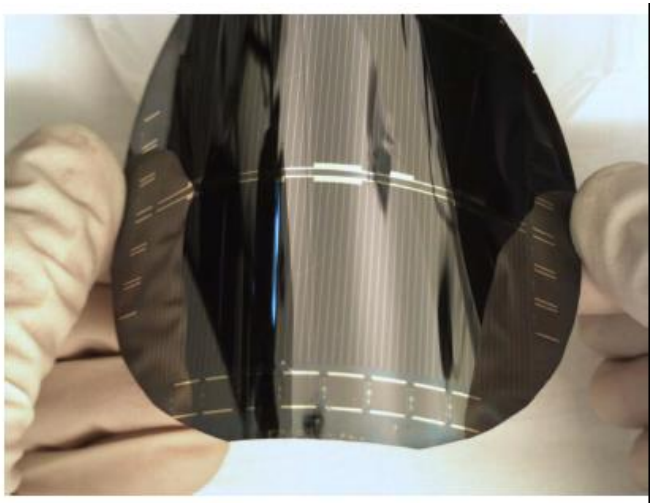
Removing the defected metamorphic region and making thin, cost-effective cells

- ❑ Grow III-V structure on substrate with release layer
- ❑ Apply flexible carrier to top of structure
- ❑ Remove release layer by chemical process
- ❑ Structure lifts off in one piece
- ❑ Transfer to temporary carrier for processing





Processed ELO Solar Cell Wafer

http://www1.eere.energy.gov/solar/review_meeting/pdfs/prm2010_microlink.pdf

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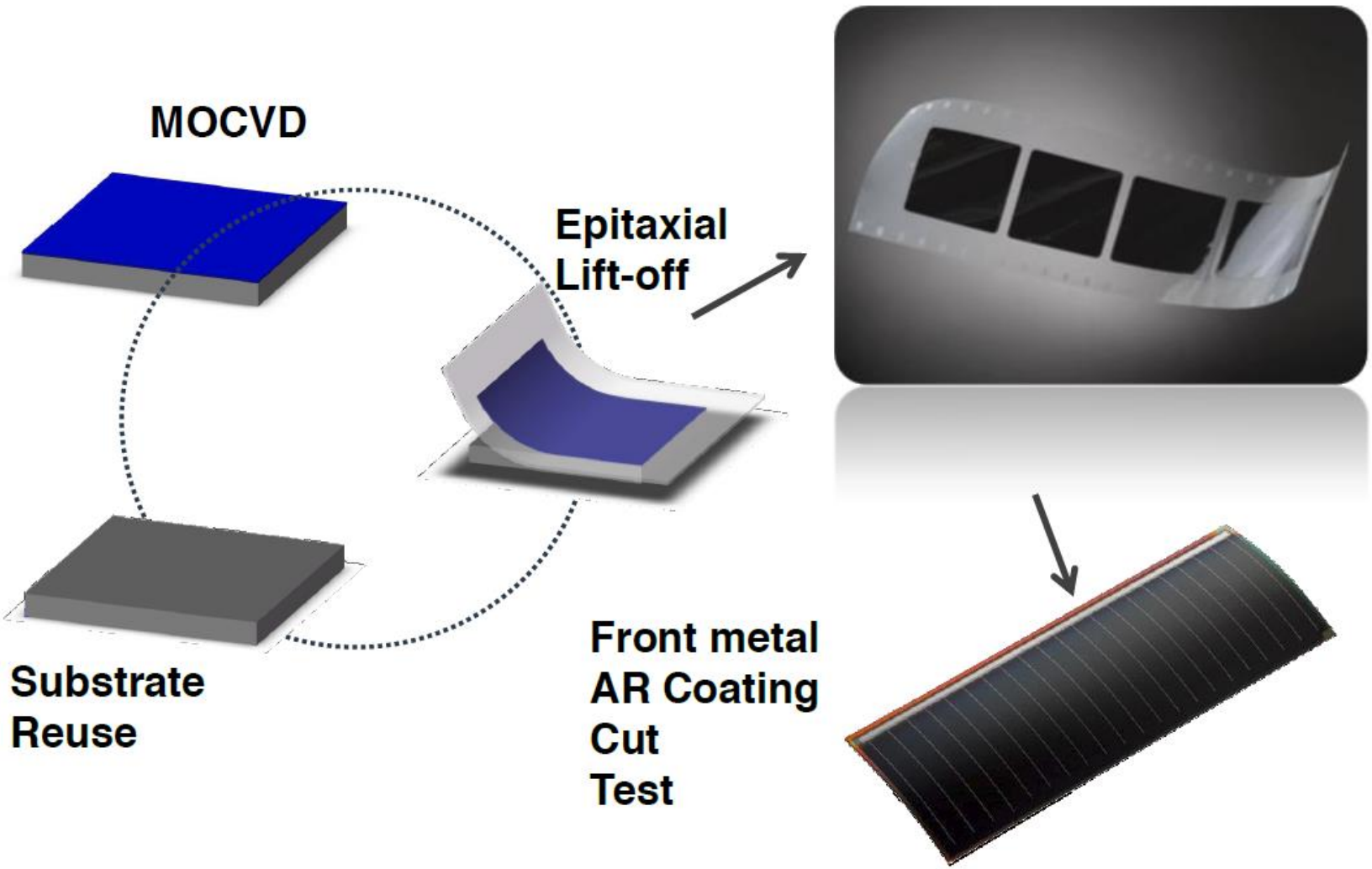
ALTA Devices: NREL PV Module Reliability Workshop, 2013



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Issues

- Excellent for flexible\low-weight applications
- Substrate reuse, without repolishing, for lower cost is an issue.

Opportunities as structured substrates

- Changing the dynamics of dislocation nucleation and propagation.
- Structured Substrates for dislocation free growth

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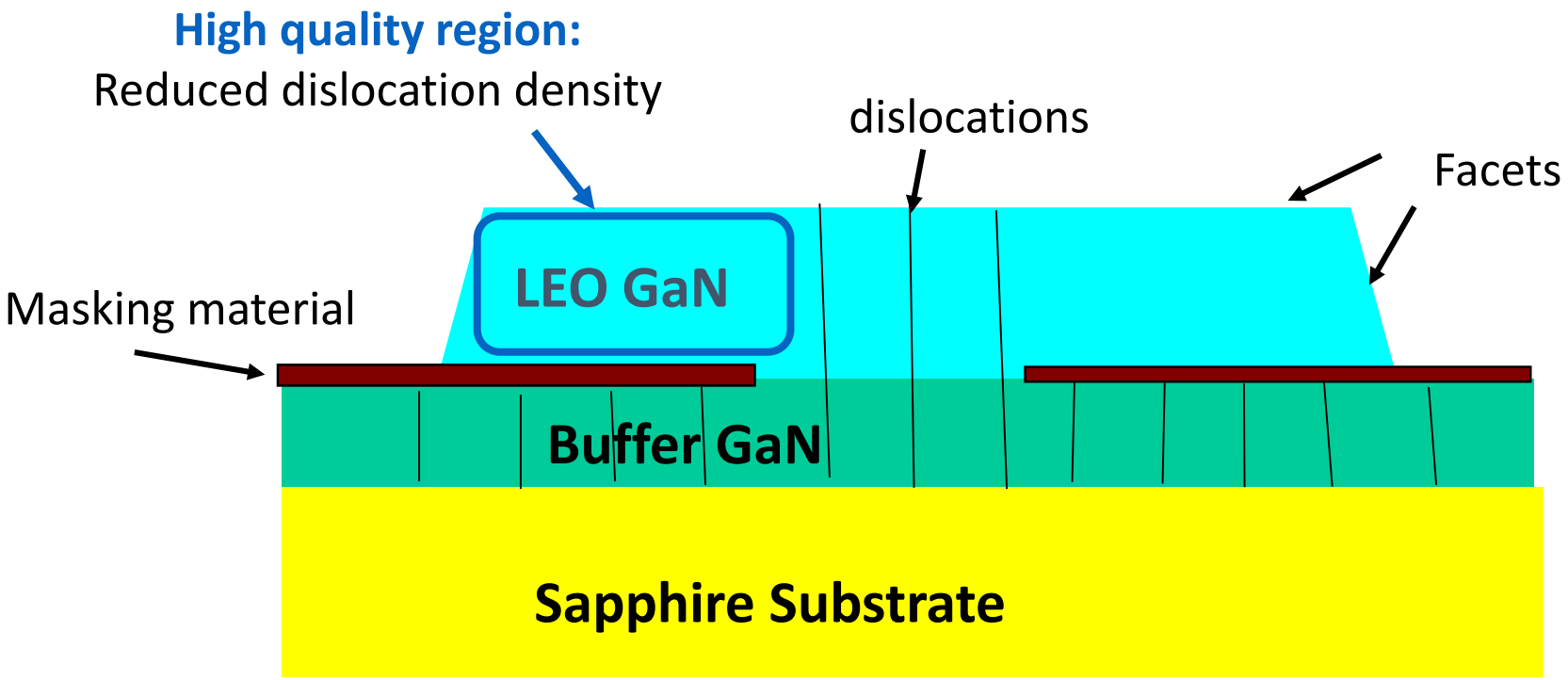
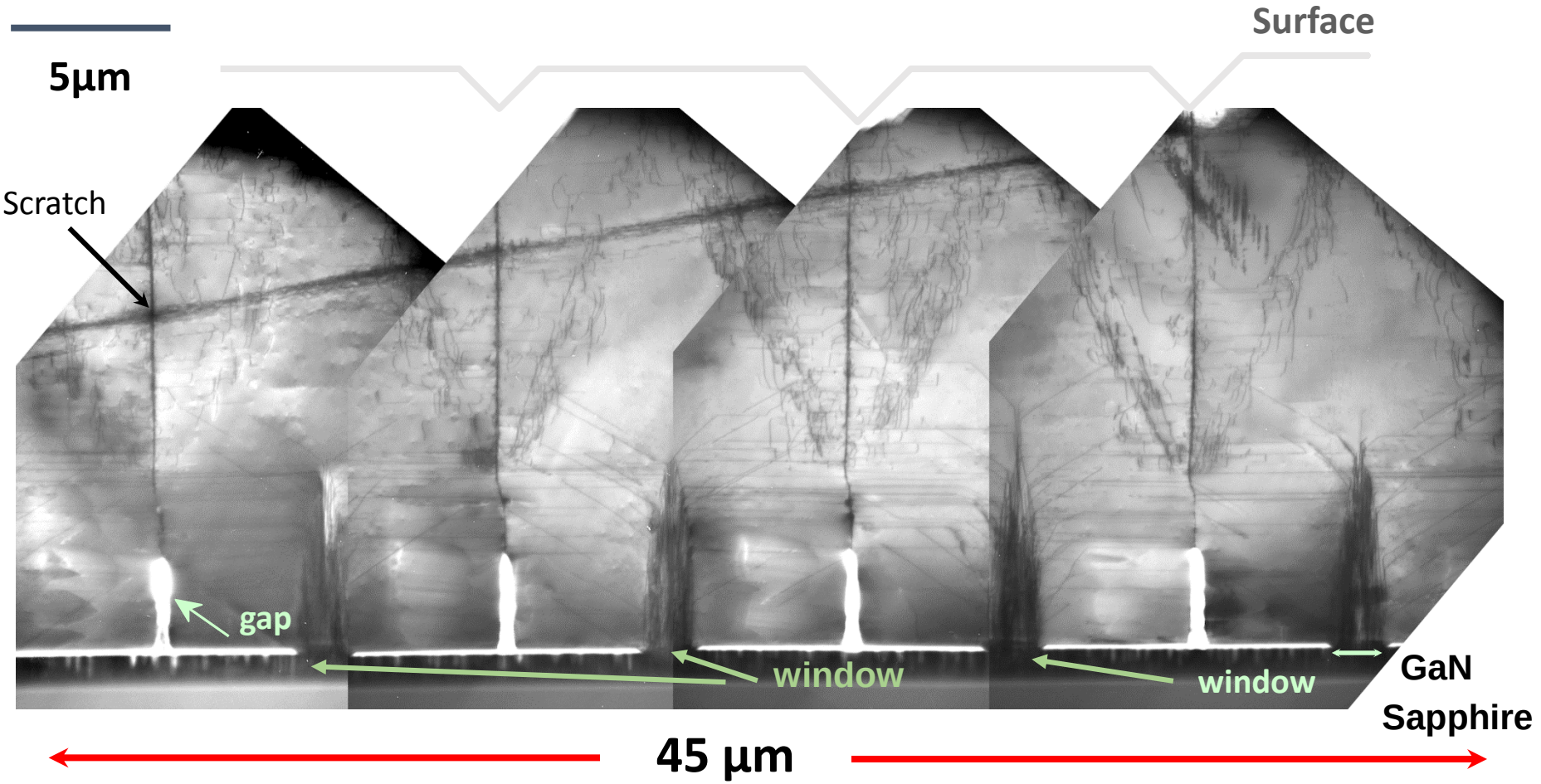
Structured Substrates: Lateral Epitaxial Overgrowth (LEO)



- **Selectivity of growth (mask versus opening)**
- **Defect Structure:**
  - **Gas phase stoichiometry**
  - **Surface energy**
  - **Strain**

TEM images on the Dislocation Arrangements within a thick LEO GaN sample



K. A. Dunn, S. E. Babcock, F. Dwikisuma, T.F. Kuech

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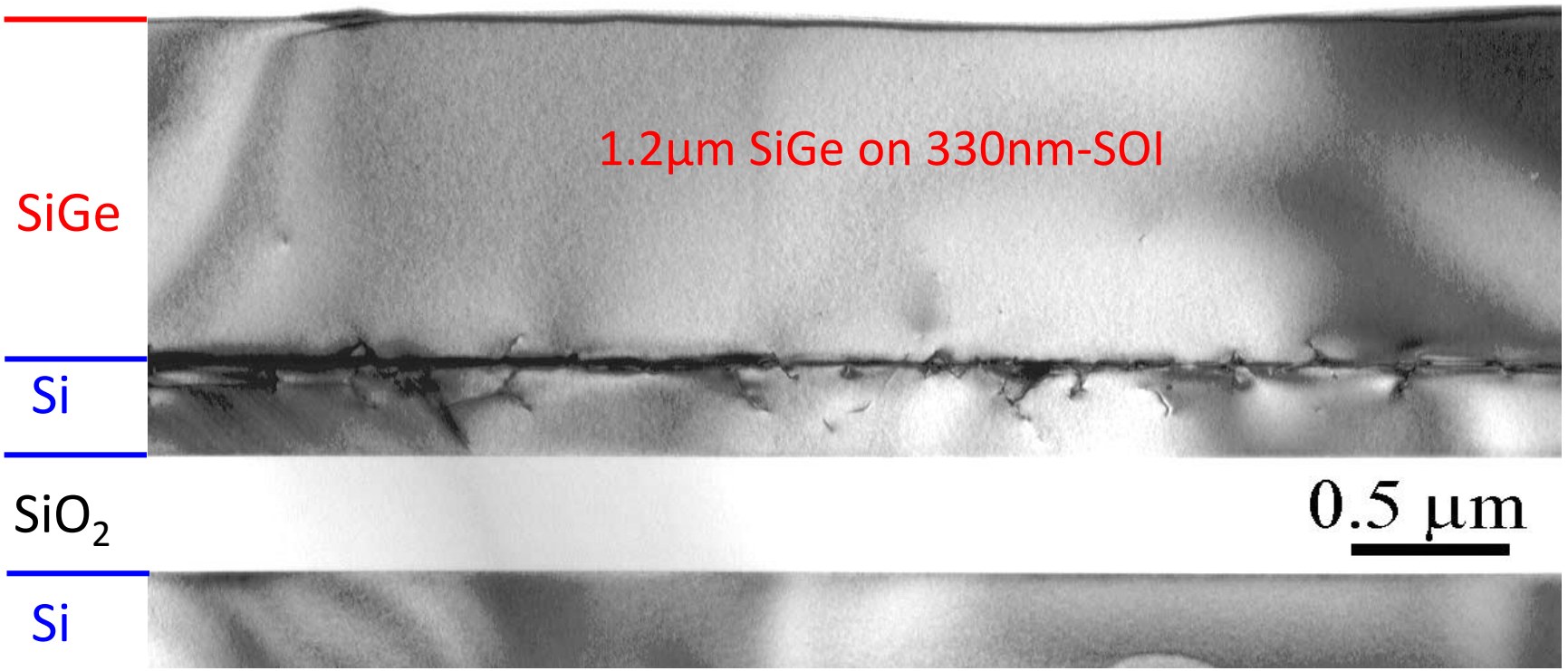
Structured Substrates: Growth on SOI
Dislocation Structure of Relaxed SiGe on SOI



- Numerous MD's at the Si/SiGe interface
- Many segments in the 330nm-SOI substrate
- No MD's at the Si/SiO_2 interface

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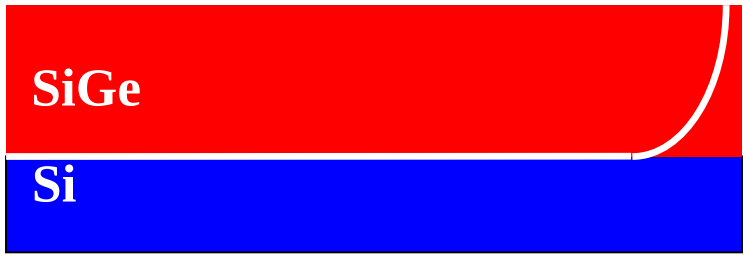
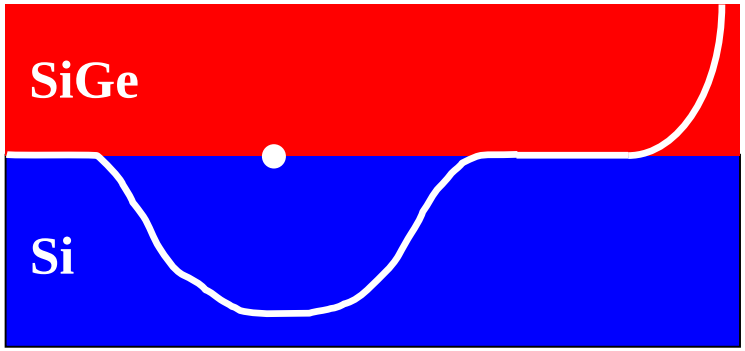
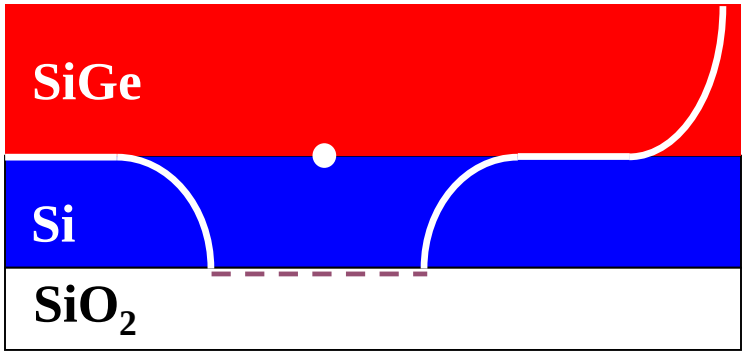
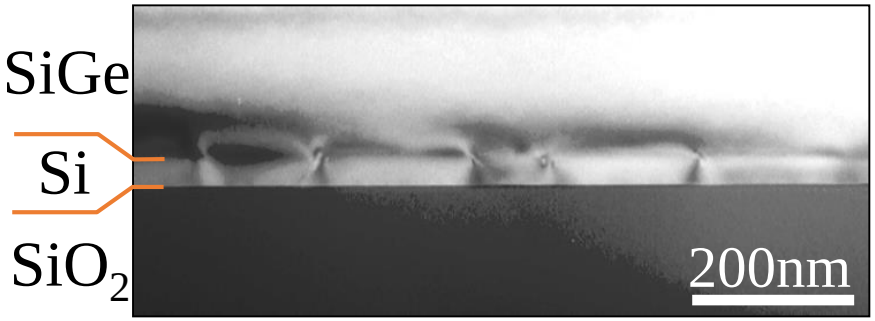
Dislocation Core-Spreading at the Amorphous Oxide









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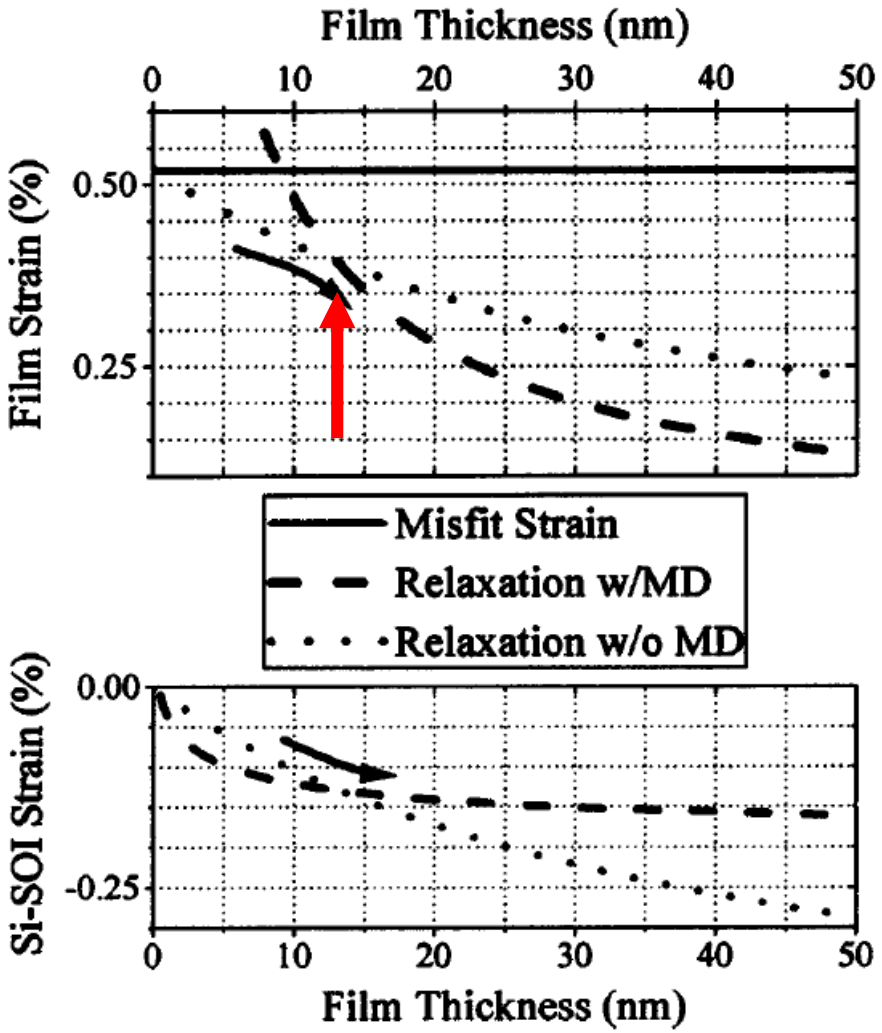
Strain as a function of $Si_{0.82}Ge_{0.18}$ film thickness on a 40 nm Si–SOI layer.



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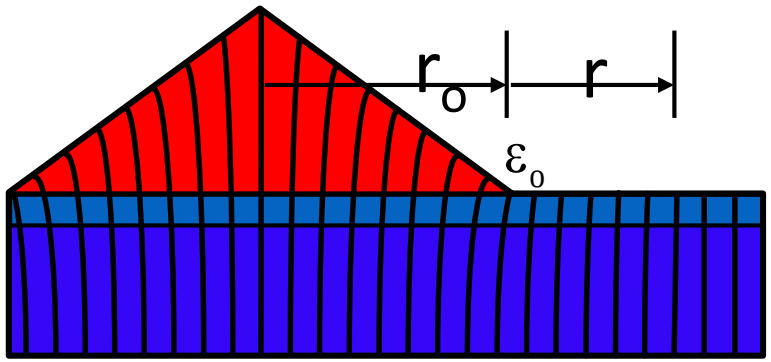
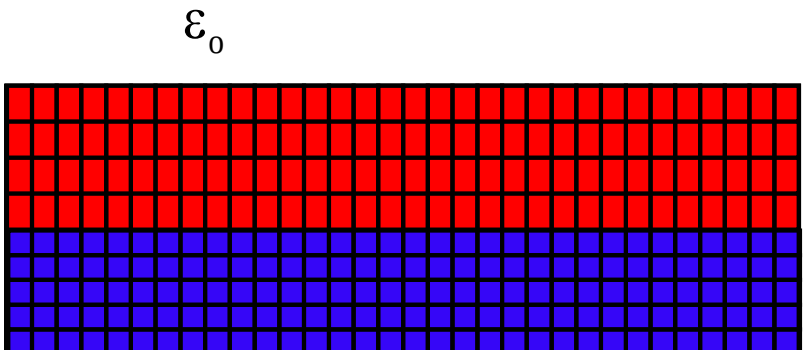
Structured Substrates – Forcing the buffer layer thickness to 'zero': Use of nanoscopic islands

Pseudomorphic islands will develop as a strain relief mechanism prior to the introduction of dislocations



Vs.



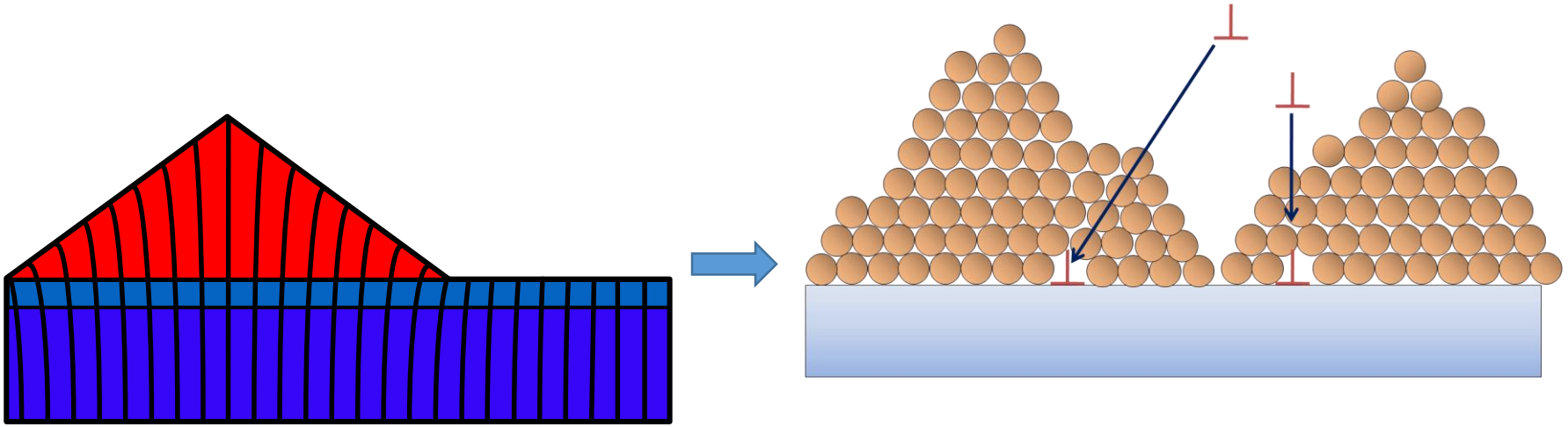
$$R \propto \exp(-\alpha\varepsilon^{-4})$$

$$R \propto \exp(-\alpha\varepsilon^{-1})$$

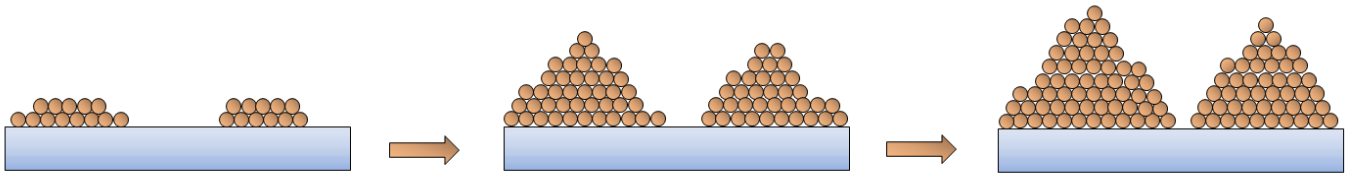
Once 'islanded', further growth leads to dislocation injection due to the increased strain at island edges.

Model of Tersoff, et al

Island Growth and Defect Formation

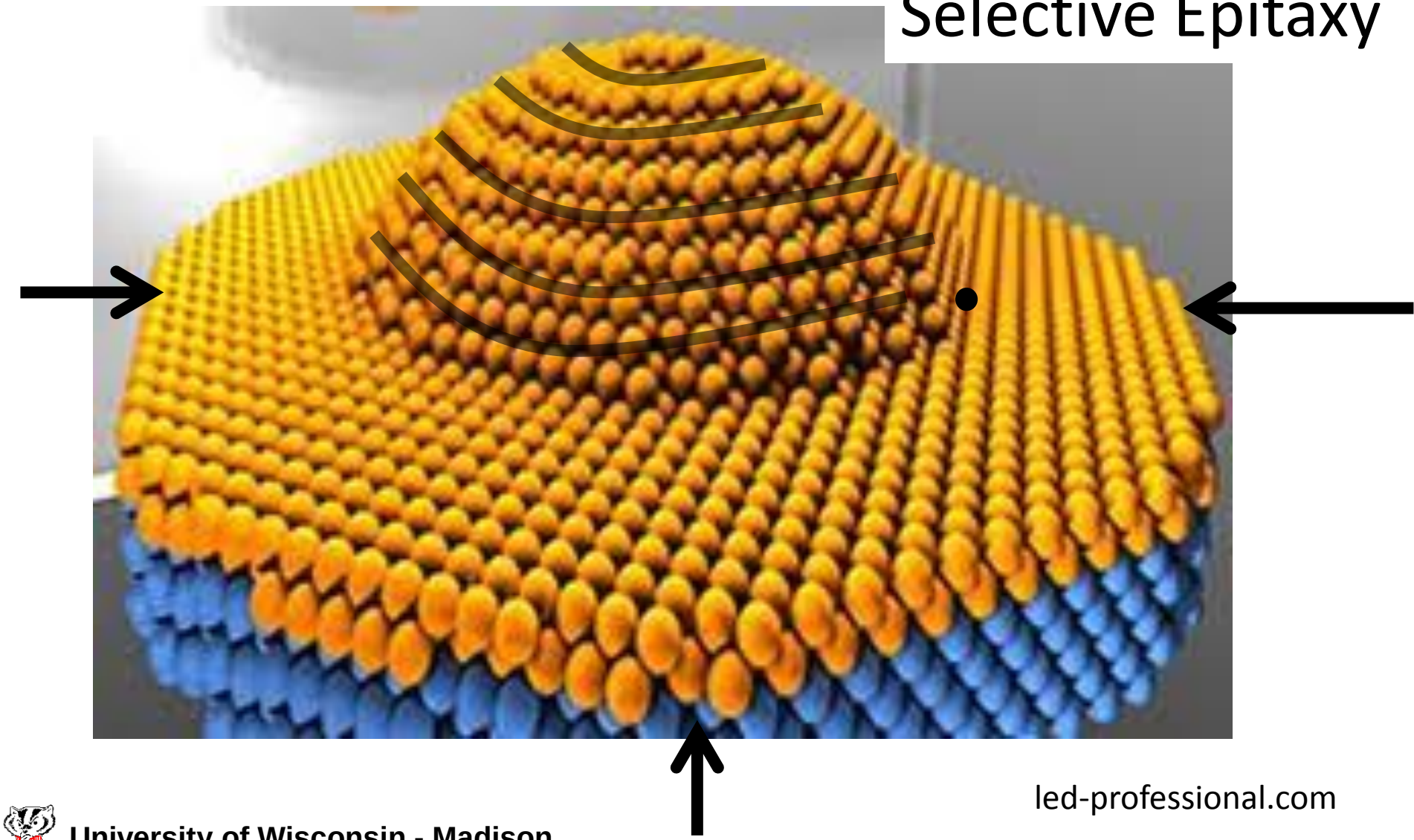


Volmer-Weber
(island growth)



Increasing Growth

Nanopatterning – what is needed?

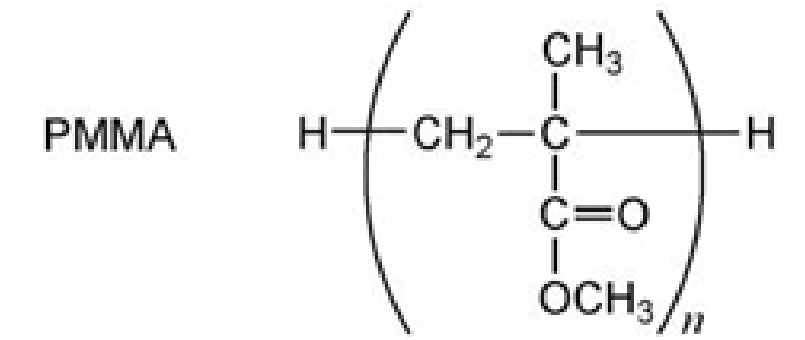


Forcing the buffer layer thickness to zero:

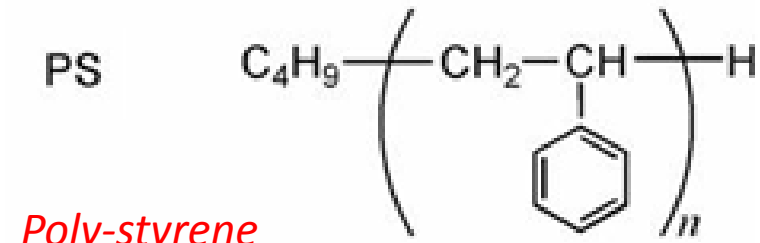
Use of nanoscopic islands

Introduce dislocations under controlled conditions prior to film coalescence

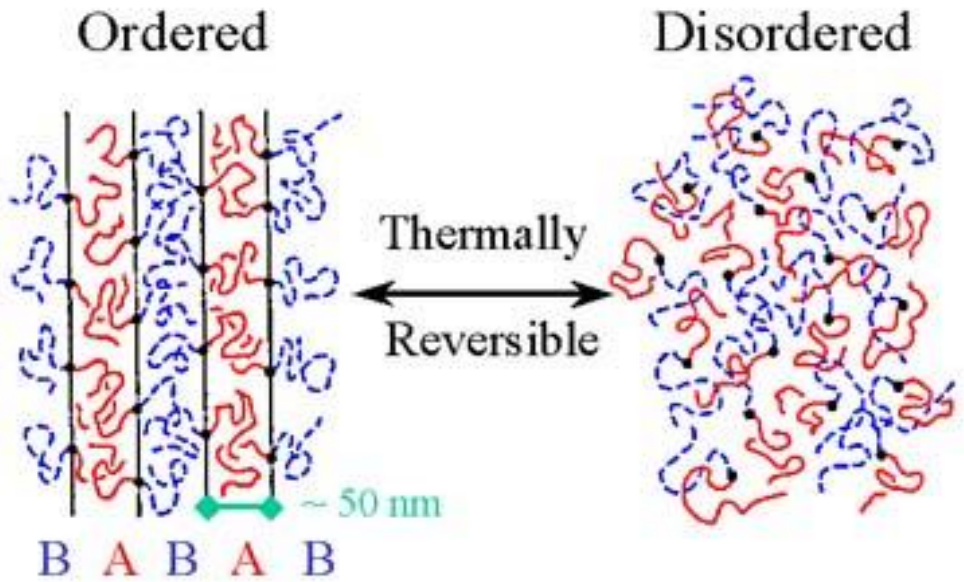
Block co-polymer: Using thermodynamics to help you



Poly-methylmethacrylate



Poly-styrene



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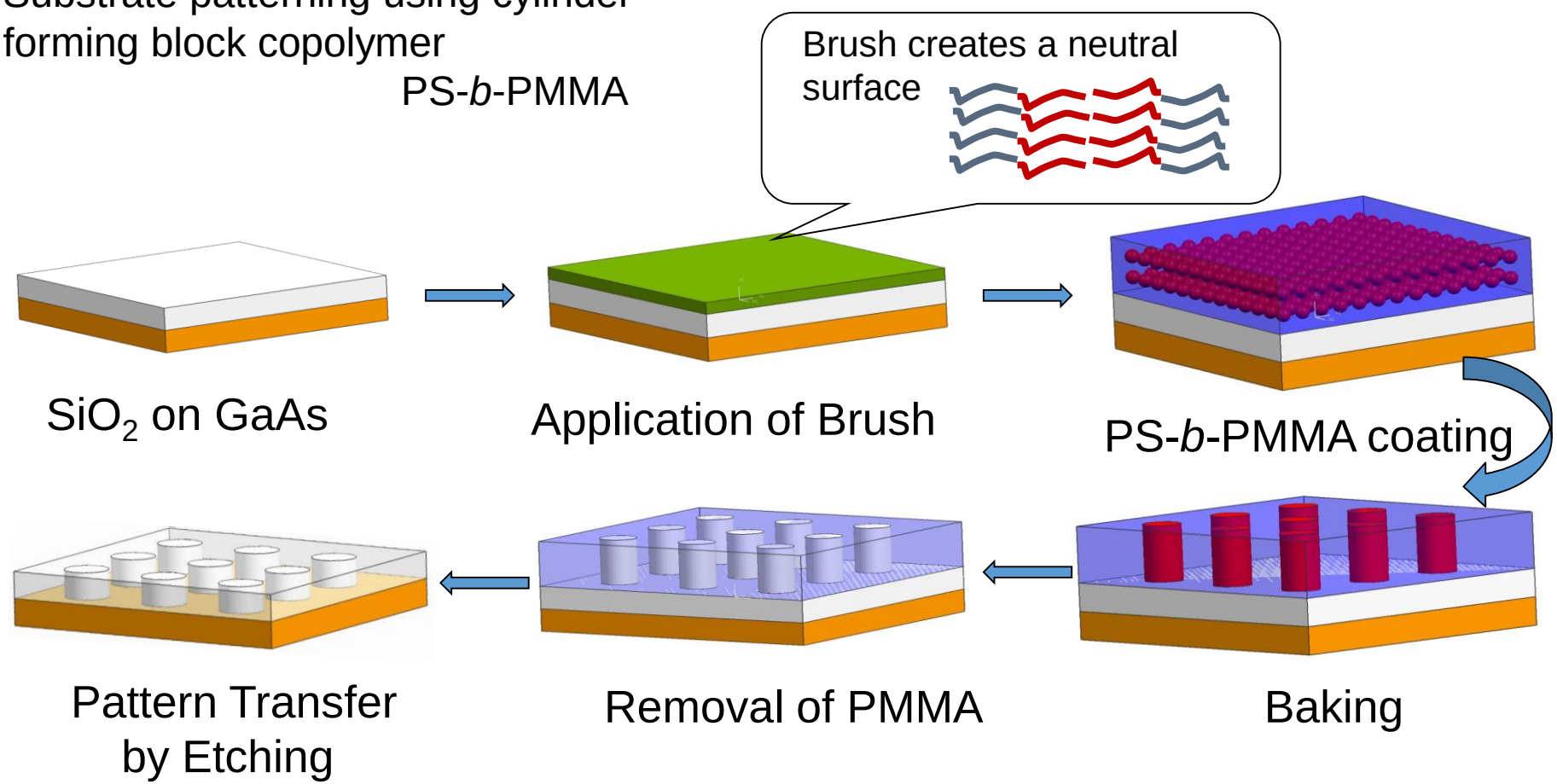
Block Copolymer-based Nanolithography to Template Growth

Substrate patterning using cylinder forming block copolymer

PS-*b*-PMMA



GaSb Growth on GaAs templates: ~8% lattice mismatch

Nano-patterned GaAs
dipped in 10% Acetic acid
~ 20 s to clean holes

↓

GaAs substrates annealed under AsH_3 for 8 mins @ Growth Temp. ~Tg

↓

GaAs buffer grown ~1 nm @ Tg

↓

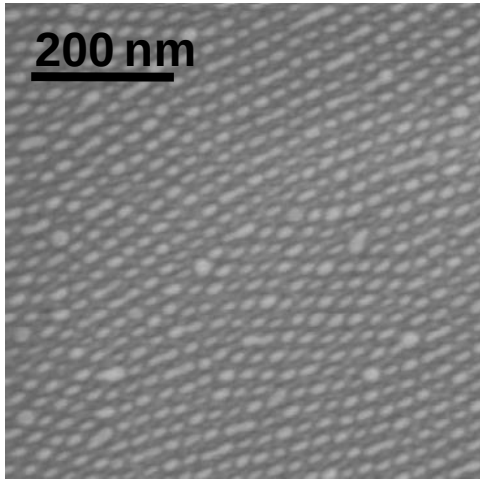
5 sec TESb pulse

↓

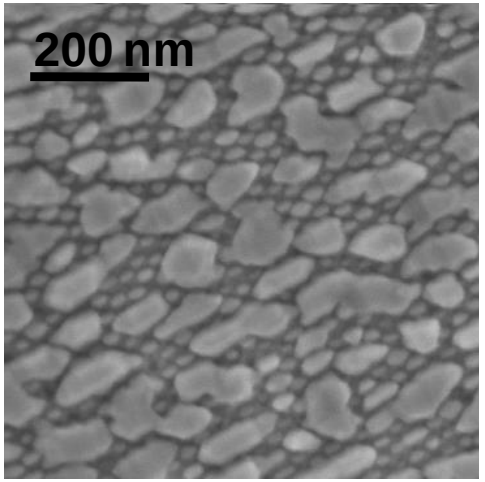
GaSb growth @ Tg

- LP-MOVPE: 76 torr
- Precursors : TEGa,TESb & AsH_3
- Substrates : {100} nano-/non patterned GaAs
- TEGa mole fraction: 6.5×10^{-5}
- Tg ~ 500 -580 °C

GaSb dots grown on nano-patterned GaAs



~18 nm GaSb



~ 30 nm GaSb

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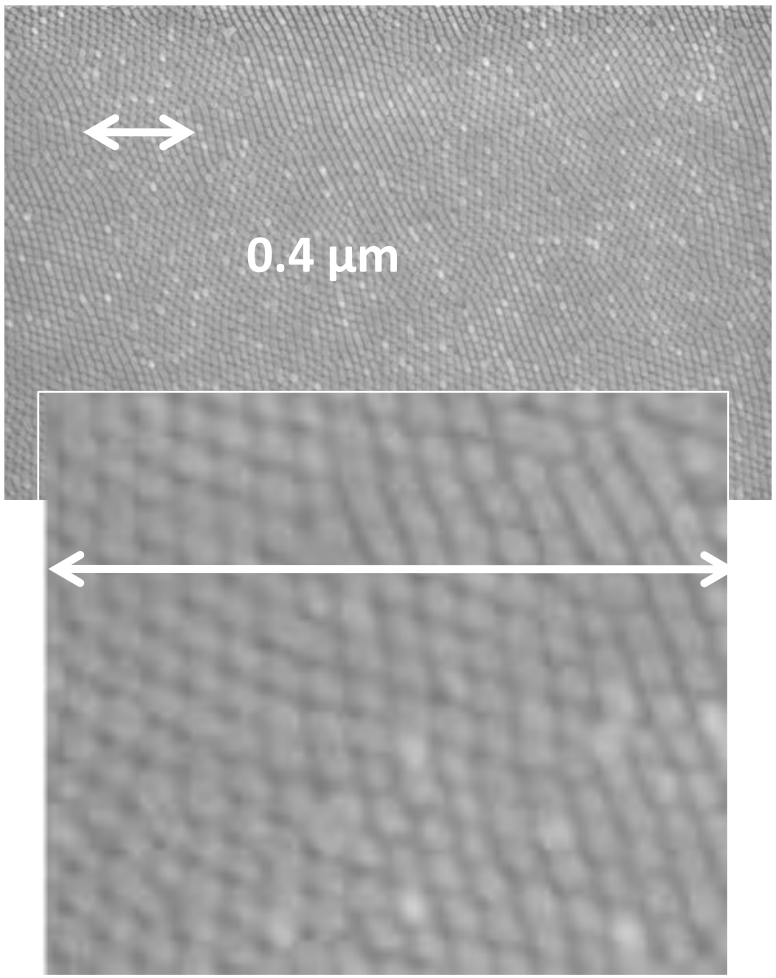
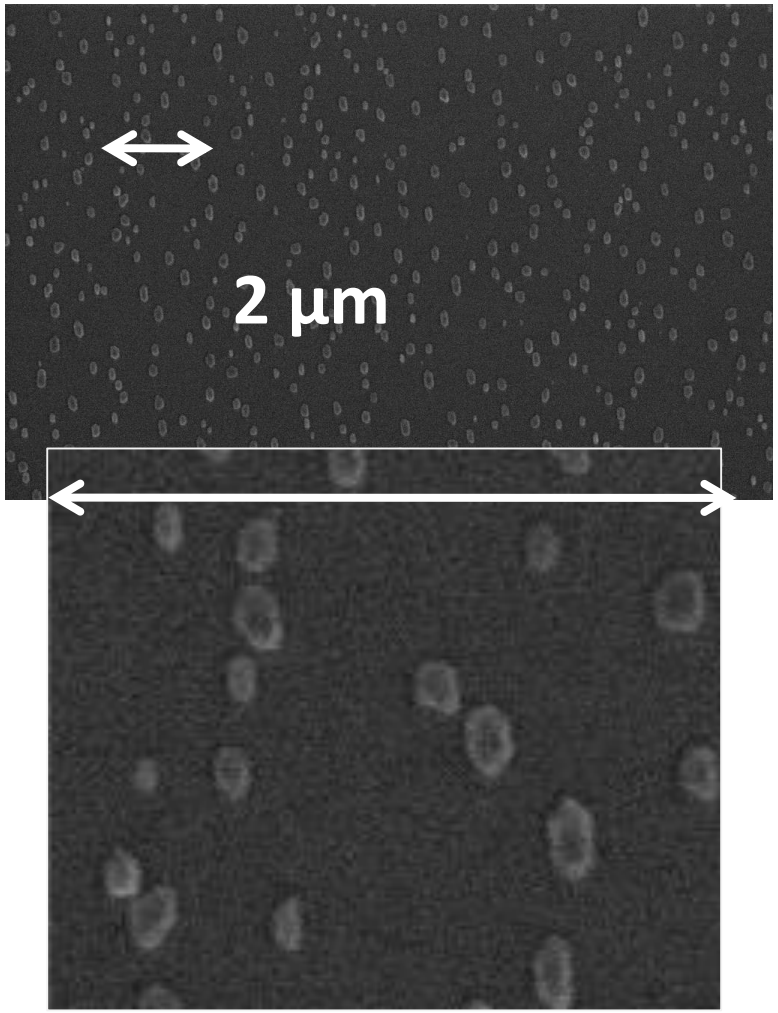
Whole Wafer Approach to Nanopatterning

GaSb on GaAs

On Oxide Pattern



On Non-patterned

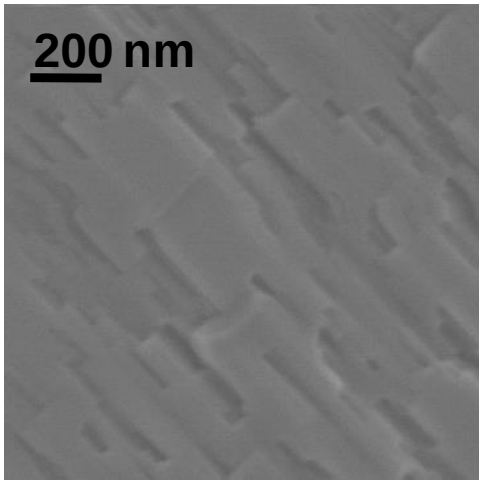


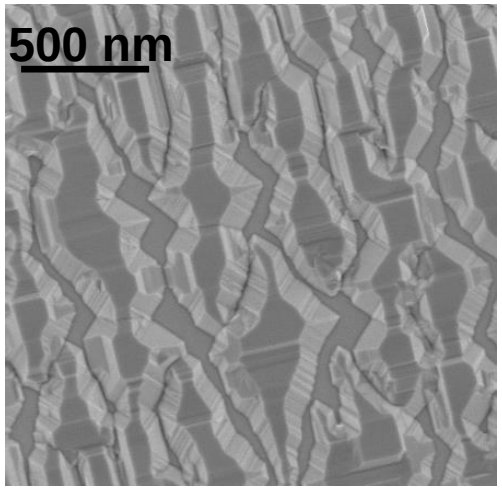
Surface Morphology

200 nm thick GaSb grown @ 530°C

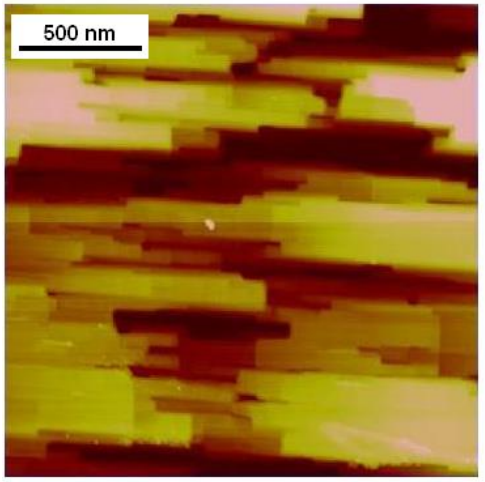
On nano-patterned GaAs

On GaAs substrate



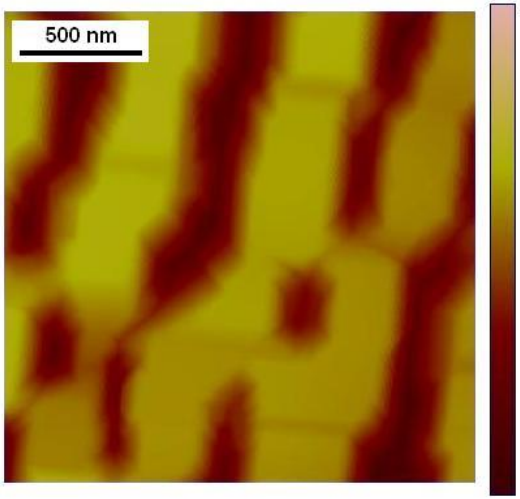


- Large islands form on non-patterned GaAs whereas film grown on nano-patterned GaAs are smooth
- On nano-patterned GaAs , GaSb growth proceeds by island coalescence @ nm scale size



20 nm

0 nm



500 nm

0 nm

RMS Roughness

On nano-patterned ~ 5.47 nm
On non-patterned ~ 71.9 nm

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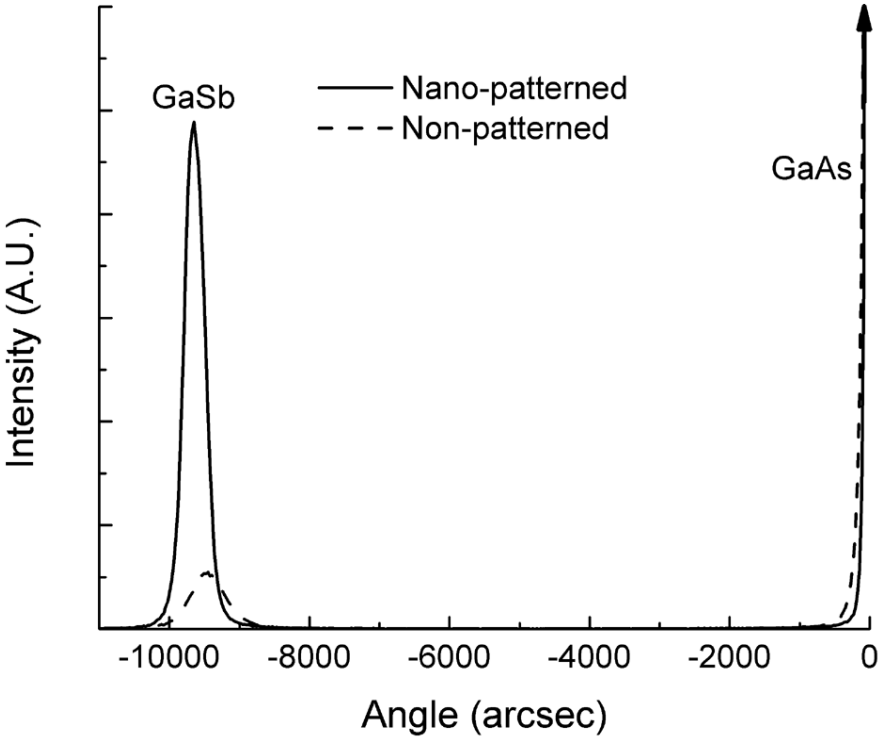

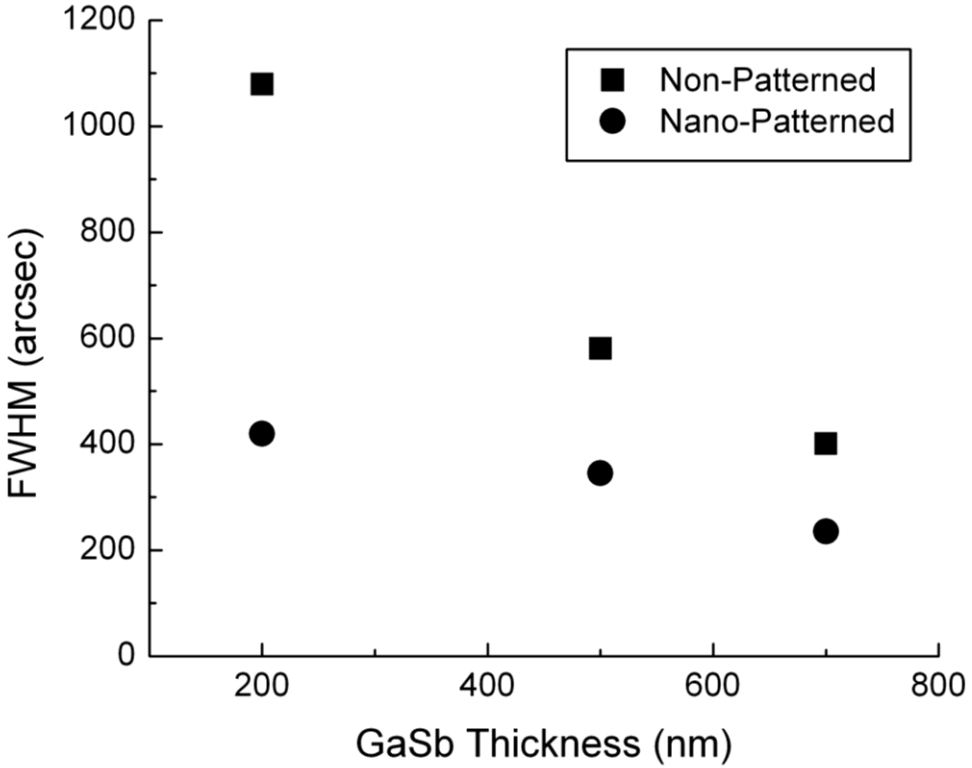

Jha, Kuech et al, Appl Phys Lett 95 (2009)

- Defect density in grown films can be assessed by FWHM of GaSb peak
- 200 nm thick GaSb film grown @ 530 °C on nano-patterned GaAs has FWHM ~420” as compared to 1076” on non-patterned GaAs
- 700 nm thick GaSb films grown on nano-patterned GaAs further shows FWHM reduction to 232”

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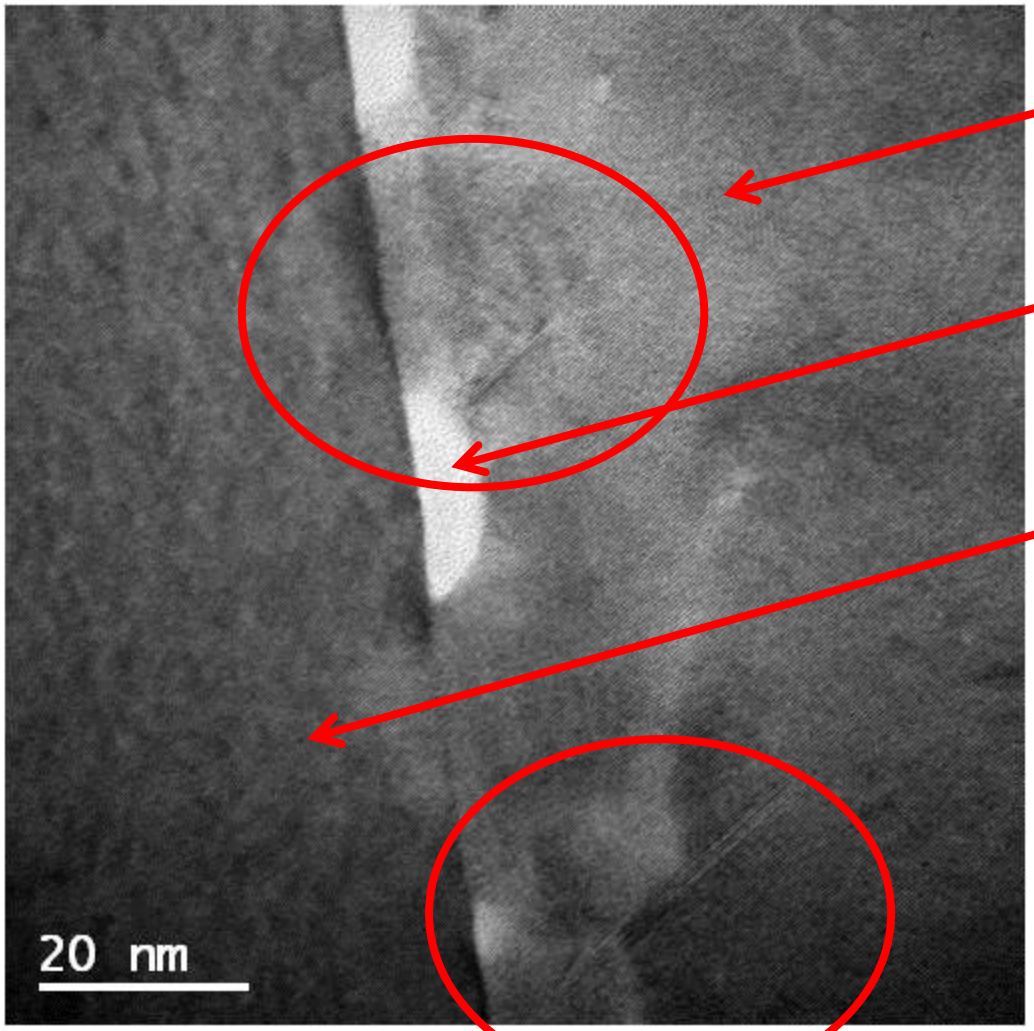
Whole Wafer Approach to Nanopatterning

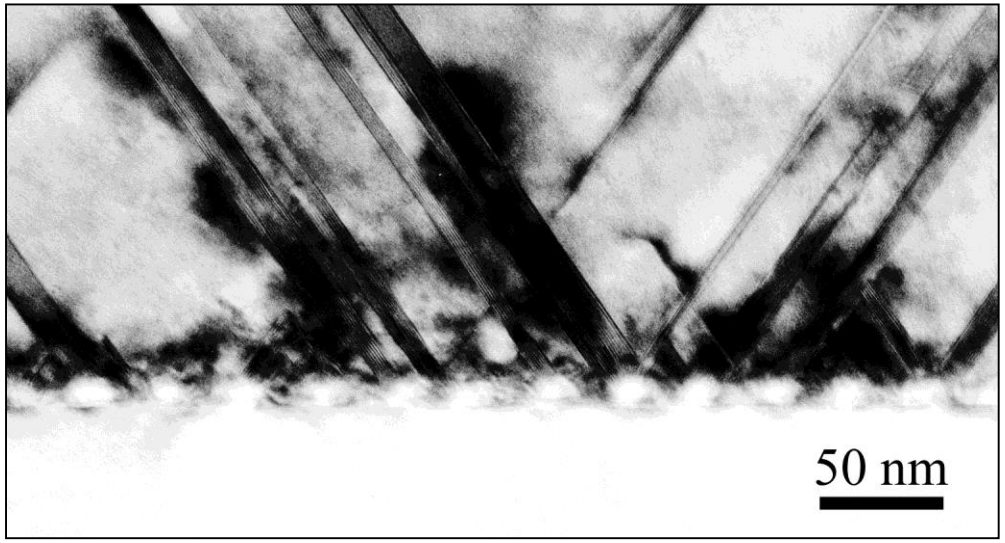


GaSb

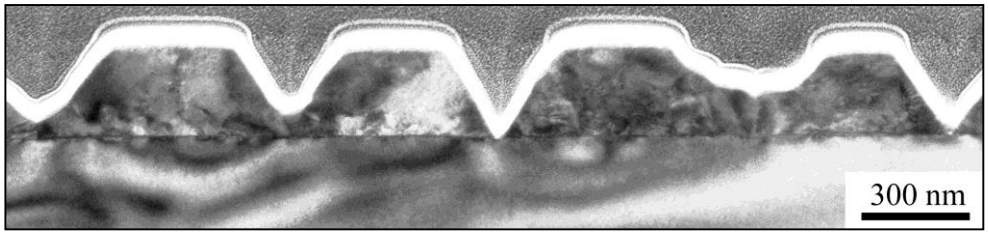
SiO_2

GaAs

TEM micrograph: Defect reduction



TEM micrograph for 200nm thick GaSb film grown on nano-patterned GaAs



TEM micrograph for 200nm thick GaSb film grown on non-patterned GaAs

- {111} twinning seen in GaSb films originate from the oxide mask
- The top surface of the GaSb film grown on nano-sized patterns is relatively defect free as seen from TEM
- Large GaSb islands can be seen for films grown on non-patterned GaAs. These islands have {111} facets and are tilted by ~ 3° relative to the substrate

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Nanopatterning – what is needed?

the film must initiate strain relaxation within the nanopattern

Surface buckling often precedes rapid dislocation nucleation

Minimum wavelength for spontaneous 'buckling': $\lambda_c = \frac{2\mu\pi\gamma}{(1-\nu)\sigma^2}$

Once emerging from the nanopattern mask, the islands compete for adatoms

- Atoms diffuse on surface sampling islands
- Attachment energy is lowest for least strained islands
- The islands increase in size creating rough morphology

$\frac{\rho_A}{J} = \tau$ and $\sqrt{D\tau}$ should be small — Low temperatures

$\frac{D\rho_A}{J}$ to restrict diffusional effects — High growth rates

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Defect Reduction by Intentional Patterning

- Strain relief by selective area epitaxy
  - Reduce threading dislocations by selective nucleation in nano-sized patterns: Threading dislocations terminate at the free edge of the pattern

- External patterning offers control over island size, density and position
  - Self assembly leads to relaxed islands with complex microstructure and high density of defects

- For effective strain relaxation pattern size of the order of diffusion length of the atoms
- Nano-patterning ~ 20 nm achieved by block copolymer self assembly

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Summary

- A large number of alternatives to direct epitaxial growth have emerged
- Specific approach depends on the device of interest
- Growth approaches
  - Metamorphic buffer layers
  - Structured substrates
  - Wafer bonding - layer transfer
- All demonstrated – transfer to commercial technology varies with approach

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Questions?

- Are we using the right materials? Can we expand the palette of semiconductors?
- Can there be a new structure/substrate to facilitate photon recycling, heat removal, ...?

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Thank you

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